Submillimeter Array Technical Memorandum

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Delay and Phase Control

Summary

This memo is an update of memo number 56, which contained a preliminary analysis of the phase and delay control for the SMA. There have been several developments in the system design, which require reanalysis of the phase and delay scheme. The revised LO scheme is significantly simpler than that described in memo 56, with only two frequency conversions between the RF and the A/D input. This is a mixed blessing, since we have had to add a small vernier delay line in the IF to replace the lobe rotator which used to be associated with the third down-conversion.

The interferometer timing has also been defined. There will be fixed synchronous timing, with a basic interval of 10 msec. The correlator design has progressed and the chunk size is increased to 80 MHz, with a spacing of 64 MHz, and 16 chunks per receiver. The phase will be switched, according to Walsh functions, in 10 μs blanking intervals at the end of each 10 msec interval. The Walsh cycles will complete every 320 msec. The correlator will be designed with DSP chips which are capable of handling 2048 point real fast Fourier transforms in 2.3 msec, justifying the original decision to handle much of the phase control in software.

I. Layout of the SMA Phase and Delay Control

Figure 1 is an updated version of the fig. 3 presented in memo #56. The current down-conversion scheme is much cleaner, with only 2 mixings. The hardware demodulation of the phase-switching has also been removed, with all demodulation being done in the DSP processors. Interleaved Walsh cycles have been chosen, rather than the nested cycles. There is a new element, a vernier delay in the IF line, which is provided to track the small delay changes during the period of one Walsh cycle. This replaces the lobe rotator associated with the old 2nd or 3rd LO.

The timing of the interferometer has now been defined. The basic period is 10 msec, during which all states will remain fixed. There is a blanking period of 10 μsec while the correlator is dumped and the lobe rotators updated, causing a loss of 0.1% in integration time. The correlator dumps will be accumulated by the DSP's into 4 buffers, one for each of the 4 phases (0°, 90°, 180°, or 270°) of the phase switch. The phase-switch will be changed each 10 msec, according to the Walsh functions, and a full Walsh cycle will be completed every 320 msec. At this point, the DSPs will perform the FFT's to calculate frequency spectra and make minor phase corrections for

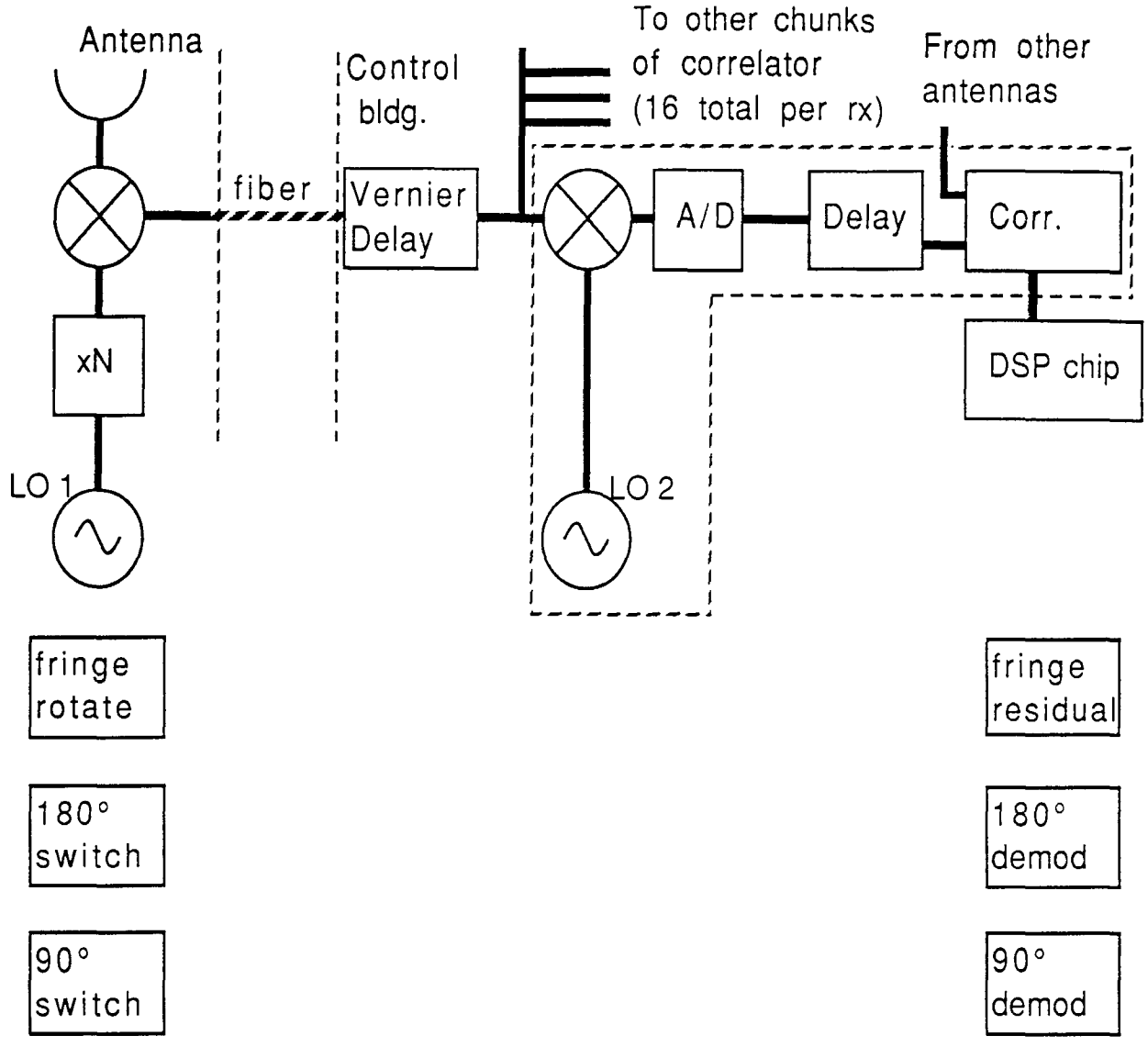

Figure 1. Frequency conversion scheme of the SMA, showing the locations of phase and delay switching elements. Only one receiver is shown. The other is similar.

fractional-bit delay errors, etc. The results of these calculations will be accumulated for a period of several seconds before being dumped to disk. The nominal period of these dumps will be every 30 seconds, but the specification is to support a rate of 1 dump every 10 seconds. Since the DSP chips (TMS320C40) proposed for the correlator boards can perform a 2048 point real FFT in 2.3 msec, so they have more than enough power to handle all of our phase control, as described in Tech Memo #65.

The basic parameters of the SMA are presented in Table 1, for the revised scheme described above. The derived parameters, such as fringe rates, are shown below this, with formulae showing their dependence on the basic parameters. I have assumed a maximum baseline of 1000 m, to handle the JCMT and CSO, with a maximum of 8 antennas and 2 frequency bands. The extension to 12 antennas is easy, either by sharing Walsh functions for the two frequency bands and keeping the

320 msec Walsh period, or by extending the vernier delay to 4 bits and the Walsh period to 640 msec.

Table I

Phase and Delay Parameters of SMA

Maximum Baseline (b)		1000 m
Min Frequency (f_{min})		180 GHz
Max Frequency (f_{max})		1000 GHz
IF Bandwidth (Δf_I)		2 GHz
Number of antennas (N)		6+2
IF chunk width (Δf_c)		80 MHz
Number of chunks	$= \Delta f_I / \Delta f_c$ + overlap	32
Delay step	$= 0.5 / \Delta f_c$	6.25 ns
Max delay	$= b / c$	3.333 μs
Max delay rate	$= 2.424 \times 10^{-13}$ b	242.4 ps/s
Max delay step rate	$= 4.828 \times 10^{-13} \Delta f_c$ b	0.0388 steps/s
Max fringe rate	$= 2.424 \times 10^{-13} f_{max}$ b	242.2 Hz
Max residual fringe rate	$= 1.212 \times 10^{-13} \Delta f_I$ b	0.2424 Hz at 1 GHz 1.454 Hz at 6 GHz w/o vernier
Dump rate limits:		
Delay smearing	$= 2.063 \times 10^{11} / (\Delta f_c$ b)	2.579 sec
Beam smearing	$= 8.251 \times 10^{3} / b$	8.251 sec
Fringe smearing	$= 4.125 \times 10^{11} / (\Delta f_I$ b)	0.32 sec with vernier delay
Interleaved Walsh Cycles		
Walsh function cycle length (90° and 180°)		32
Walsh cycle period		320 msec
correlator dump time		10 msec
Fourier transform time		320 msec

II. The Vernier Delay

In the scheme described in memo #56, a lobe-rotator was applied at the third frequency conversion, permitting the fringe rate to be set to zero at the center of the IF band. Despite the presence of this rotator, the residual fringe rate at the edges of the IF band (+/- 1 GHz from the center) was the dominant driver of the Walsh cycle time, which was limited to 0.412 sec at a baseline of 500 m, or 0.206 sec at 1000 m. Since we now have no third LO and no associated lobe rotator, the residual fringe rates are increased and the maximum residual rate is found at the top of the IF band (6 GHz), and the Walsh cycle time would be limited to .034 sec.

For practical reasons, it is hard to dump the correlator much faster than 10 msec. The total number of Walsh functions needed to handle 2 receivers, 8 antennas, and quadrature switching, is 32, giving a minimum Walsh cycle time of 320 msec. This is an order of magnitude greater than the 0.034 sec limit set by the residual fringe rates, and it is necessary to provide some hardware method of reducing the residual fringe rates.

Four possible ways of doing this were considered. The first was to add another frequency conversion as in the original scheme, purely to allow the phase to be changed. A second possibility was to add lobe-rotation to the baseband converters, but this required a large number of new synthesizers. The third approach was to apply offsets to the timing of the samplers, but this also complicated the design. We therefore chose the fourth approach, a short vernier delay line, which is fairly simple, and performs better than the originally proposed lobe rotator.

This vernier delay is a short length of delay line in the IF line of each antenna, which can track delay changes during each 320 msec cycle. At the end of each 320 msec cycle, the vernier is reset to the end of its range so that it can track the delay changes during the next period. Therefore only a short length is needed, just enough for the maximum change of delay during any 320 msec cycle. The gross delay is still removed by the digital delay line, with fractional-bit compensation in software in the DSP's. Since the vernier provides a delay rather than a phase, it corrects the fringe phase exactly all across the IF passband, unlike the originally proposed lobe rotator which could correct the phase only at one frequency.

Since the delay has to be compensated only for the duration of one Walsh cycle (320 msec), the delay line can be very short, 0.2424 (nsec/sec) x 0.32 (sec) = 77.57 psec for 1000 m baseline. This corresponds to a path length of 2.3271 cm in free space or about 1 cm of strip line. As before, we should try to minimize losses due to delay errors in this part of the system. To keep losses to less than 0.4%, the resolution should be better than 1/20 wave at the highest frequency in the IF, or 8.33 psec. A total of 9.3 steps are then required to cover the whole range of 77.57 psec. The total delay on any baseline is the sum of two separate delays in two antennas, so each antenna should have half the range, with steps 0.707 times smaller than 1/20 wave (5.9 psec). This leads to a 3 stage binary delay line in each antenna, with a step size of 5.5 psec, and a range of 38.5 psec. At the maximum rate, the delay would run through the 8 states in a 320 msec cycle, and the vernier delay would have to be adjusted every fourth 10 msec period.

When the vernier delay is used, the duration of the basic Walsh cycle is limited only by the length of the delay line, since there is zero residual fringe phase across the IF band. In the earlier case, with the fringe phase corrected only at one frequency in the IF, the duration was limited by the the uncorrected phase at the edges of the IF band. This means that the duration of the Walsh cycle could be increased, if necessary, by increasing the length of the vernier delay until some other limit is reached. It is unlikely that we will need to do this, but it is a useful backup in case there is some problem with processing in the correlator, and it provides options in the case of expansion of the array.

There are several practical details in the delay system which must be considered. We can tolerate rather large errors in the delay values (~1/2 step), because the steps are already specified to be very small. However, amplitude variations associated with the delay changes could give spurious signals at the correlator output, so some care must be taken to balance the switches, or to provide ALC.

III. DDS Considerations

The only lobe rotator in the new system is the Direct Digital Synthesizer (DDS) in each antenna. At the beginning of each 10 msec period, this is set at a new starting phase and phase rate. The maximum phase rate is determined by the maximum fringe frequency for that antenna relative to our reference position. If the reference position is chosen to be in the center of the array, the maximum rate for any antenna relative to the reference is 121 Hz. However, if we set the reference point at one of the outer antennas (e.g. CSO), the rate at the other antennas could be as much as 242 Hz.

We will operate by setting an initial phase at the beginning of each 10 msec cycle, along with a rate which applies during that period. It is easy to show that the variation in rate during any 10 msec period is small enough that our linear approximation to the phase is adequate. The maximum fringe frequency on any one baseline, p_{max} , is given by

$$p_{max} = f_{max}\, \tau_{max}\, dH/dt \qquad \text{Hz},$$

where f_{max} = 1000 GHz is the maximum operating frequency of the SMA, τ_{max} = 1000/c is the maximum delay between two antennas, and dH/dt = 7.27×10^{-5} rad/sec is the rate of change of Hour Angle with time. The maximum change of fringe frequency with time, $(dp/dt)_{max}$ is given by

$$(dp/dt)_{max} = f_{max}\, \tau_{max}\, (dH/dt)^2 \qquad \text{Hz/sec.}$$

These equations give values of 242 Hz for p_{max}, and 0.0176 Hz/sec for $(dp/dt)_{max}$. In a 10 msec period, the maximum error due to (dp/dt) is given by

$$\phi_{max} = 360 \times 0.0176 \times (0.01)^2 \quad \text{degrees}$$
$$= 6.34 \times 10^{-4} \quad \text{degrees.}$$

There is an important detail in setting the phase of the DDS. To maintain coherence losses to 0.1%, the phase errors due to resetting of each DDS must be less than 0.022 radians or 1.28 degrees. Since the DDS output frequency is 9 MHz, the timing of the updates must be held accurate to 0.40 nsec, which is a very small value. In practice, the DDS is driven by a clock at ~50 MHz, and the relevant requirement is that the phase should be set at a repeatable clock cycle in each antenna, so that the phase difference between antennas will remain fixed. This entails adjustment of timing to ensure that the 10 msec pulse has a well-defined, stable relationship to the DDS clock.