# Harvard–Smithsonian Center for Astrophysics

Harvard College Observatory

Smithsonian Astrophysical Observatory

# Submillimeter Array Software/Technical Memorandum

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From: Raymond Gonzalez, Robert Calder, Martin Levine

## *Software Control and Hardware Addresses for the SMA*

### Abstract

The architecture for the task as well as the PMAC, DPRAM, SHRMEM and other hardware interactions are described. Please refer to the glossary for acronym definitions.

### The VME backplane data buffer and the ACCx Shared Memory

Each antenna will have an ACCx with a VXI-MXI interface card on a VXI crate, five(5) PMACs (maybe 6) with a MXI interface and support cards on a VME crate. Each PMAC will have 16Kbyte segment of DPRAM which will total 81Kbyte of DPRAM for 5 PMACs. There well be 1Mbyte of address space on the VME backplane, which means that the VME will have 966Kbyte space left over for future development(fig. 1). All data from DPRAM will be visible on the VME backplane.

There will be a one to one relation between the SHRMEM and the VME backplane, except that SHRMEM will keep its value in words(4*8bits). There will be six(6)(maybe 7) memory segments with one(1) continuous piece of SHRMEM. One(1) segment for each PMAC and one(1) for other hardware. SHRMEM will start at zero(0) and continue to 24576. Information will be refreshed in SHRMEM by functions that peek and poke at the VME backplane(fig. 2). When data has been retrieved the functions will set a flag so that PMACs DPRAM can refresh the VME address space. For more information refer to SMA Tech Memo #75.

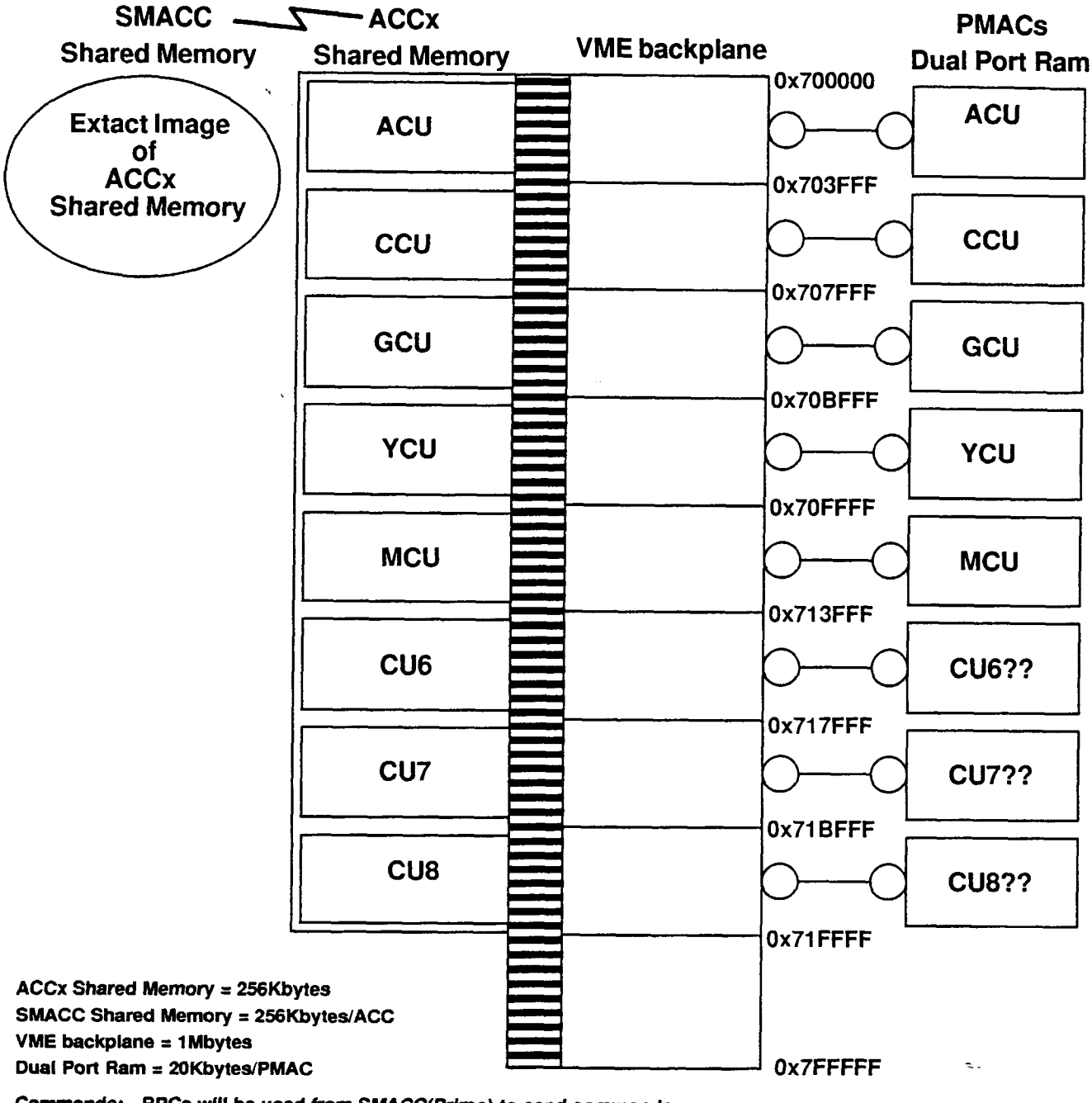
### Addresses for antenna hardware

These addresses were established so that confusion would not arise later in the project. Some formal way of adding or giving addresses was needed for the sake of keeping record, and developing the include files needed for the project. There might be some hardware not given addresses as of yet. This is NOT due to error or forgetfulness, but due to how the project is progressing. Enough room was left on the VME backplane to accommodate more PMACs as well as other non-PMAC items.(TABLES for VME backplane and SHRMEM)

### ACCx Operating System and software

As has been mentioned since the beginning of the project(SMA Project Book-SAO Memo. P. Bratko, A. Stark), the SMAs choice of operating system will be LynxOS.(Tech. Memo. Report #78, Project Book, Glossary). There will be five(5) to six(6) tasks filtering data from the VME backplane to SHRMEM on ACC1 - ACC6. SHRMEM segments will be called VMEACC1(antenna 1) - VMEACC6 (antenna 6), A list of task names are given in Appendix A.

# PMACs Dual Port Ram to ACCx Shared memory data flow




**ACCx Shared Memory = 256Kbytes**
**SMACC Shared Memory = 256Kbytes/ACC**
**VME backplane = 1Mbytes**
**Dual Port Ram = 20Kbytes/PMAC**

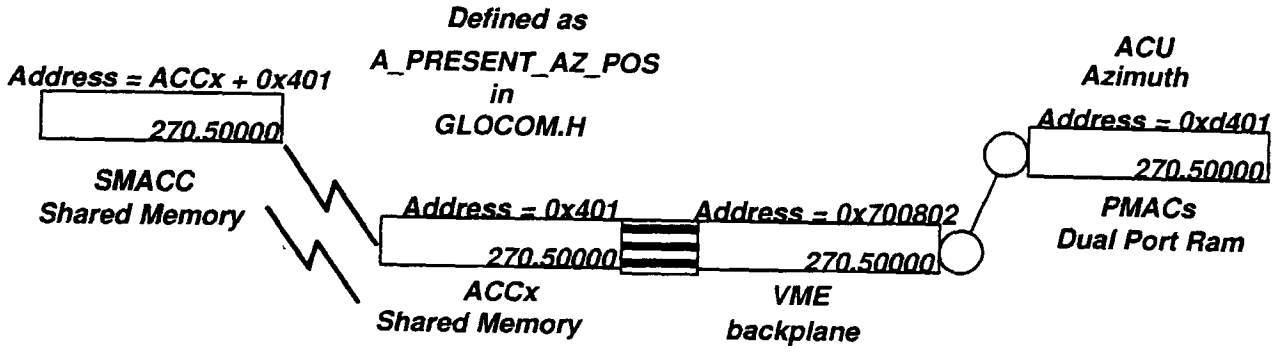
**Commands: RPCs will be used from SMACC(Primo) to send commands.**

*– fig 1 –*

# Following a value from PMAC hardware to SMACC

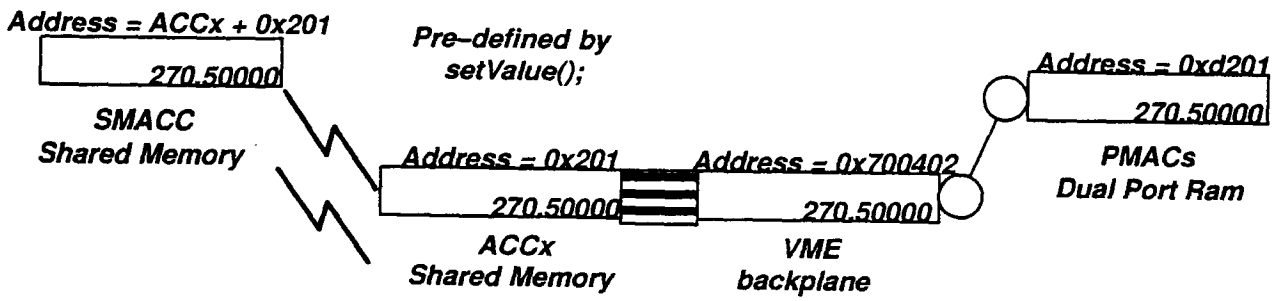
## Get Current AZIMUTH Value:

*To retrive a value via PMAC->VME->SHRMEM the function getValue() is used.*
*getValue(ACU, A_PRESENT_AZ_POS);*




## Send an AZIMUTH command:

*To send a command to the Hardware via SHRMEM->VME->PMAC.*
*setValue(AZ, 270.50000);*




– fig 2 –

## Appendix A.

***Here are some routines for getting data out of SHRMEM and sending commands. Routines for filling the SHRMEM are also listed.***

- getValue(from, address)
  - (from) can be ACU, YCU, G.. or OTHER etc.
  - (address) is the location of the data in SHRMEM.
- setValue(what, value)
  -(what) who do you want to command AZ, EL, LO1 .... etc.
  (what will be pre-defined inside setValue).
  -(value) what do you want to commanded to.
- dpracu, dprccu, dprgcu, dprycu, dprmcu, dprcu6, dprcu7, dprcu8
  - each fill there section of SHRMEM.
  - they will more then likely be started at bootup in the final system.

***Here are some routines need for communication via serial line, and VMEbus. Some routines for synchronization of SMA1, SMACC, ACCx and PMACs.***

- pm
  - a serial communications routine(driver) to talk to a selected PMAC via the serial port(COM2) on ACCx.
- vxibus
  - switches interrupt who
  - (example: vxibus 2 2 ) the first 2 is interrupt 2, the second 2 is PMAC number 2 on the VME.
  - communicates via the mailbox registers on the VMEbus.
- vxidpr
  - switches interrupt who
  - (example vxidpr 2 2) same as vxibus.
  - communicates via DPRAM on the VMEbus.
- rdate
  - switches -d host
  - (example rdate -d cfara1) show me the time and date cfara1 has.
  - (example rdate cfara1) get time and date from cfara1 and set the calling host.
  - used to synchronize all ACCx's to SMACC, until NTP is available.
- syncAllPmacs
  - synchronize all PMACs servo timers to the ACCx clock.

### *ACCx (Antenna Control Computer):*

Computer for controlling antenna hardware.

- 486DX2-50Mhz.
- 8Mbytes RAM.
- TCP/IP, NFS, STREAMS.
- 240Mbytes of IDE-Hard Drive storage (This may or may not be used, but it's there if we need it).
- Lynx Operating System version 2.2.

### *DPRAM(Dual Port RAM):*

The 8K x 16bit dual-ported RAM option is a nice addition to the PMAC-VME card since if provides high speed data exchange between PMAC and the VXI-VME ACCx over the VMEbus. Data may be written to and read simultaneously by the PMAC-VME and the VXI-VME ACCx. One main advantages of using dual-ported RAM is that it allows extremely high speed acquisition of data by the ACCx

### *Hard-RT(Hard Real-Time):*

Microsecond to millisecond reponse times.

### *LynxOS(Lynx Operating System):*

LynxOS is a real-time re-implementation of UNIX. LynxOS looks like UNIX from a user/programmers point of view. However, LynxOS was written from scratch with deterministic, high-performance real-time responsiveness for real-time applications, while still managing to look pretty much like a UNIX system. LynxOS supports a lot of facilities necessary for real-time operation:

- ROMability
- Kernel configurability to small sizes.
- Deterministic response times even when multiple devices are interrupting.
- Priority-inheritance and priority-ceiling-capable semaphores.

### *MXI(32bit Multisystem eXtension Interface bus):*

This card (VXI-MXI or VME-MXI) is used to extend an existing VME/VXIbus system to another VME/VXIbus crate.

### *PMAC(Programmable Multi-Axis Controller):*

A very flexible controller, that takes up two(2) slots in the VME create. This card is suitable for many different types of applications, with different types of hosts, amplifiers, motors, and sensors. It also has the ability of running Hard-RT tasks as well as Background tasks. Most Hard-RT programs will run in this card, leaving the ACCx almost free of any Hard-RT time duties.

### *RB(Rotary Buffer):*

The rotary motion program buffers allow for the downloading of program lines during the execution of the program and for the overwritingof already executed program lines. This permits continuous

execution of programs larger then PMACs memory space, and also RT downloading of program lines.

### *RT(Real-Time) or RTOS(Real-Time Operating System):*

RT is the actual amount of time consumed by an operation, rather than just the amount of computer time. RTOS is an operating system that is both task deterministic and works on a task priority basis, with very fast interrupt latency, context switching and task response times.

### *SHRMEM(Shared Memory):*

SHRMEM is used as a mechanism to map the monitor and control registers of the PMAC into user memory. This makes the PMAC and other hardware easy to monitor and control with user-level software, and SHRMEM makes it easy to transfer data to any other host.

### *SMA(Submillimeter Array):*

The history and scientific goals as discussed in the "Design Study for the Submillimeter Interferometer Array of the Smithsonian Astrophysical Observatory" (February, 1992).

### *SMACC(Submillimeter Array Control Computer):*

Computer for monitor and control of SMAs 'n' element array. This will also be used as the monitoring system for the correlator(Backup for SMACC only has 500Mbytes of IDE storage).

- 486DX2-66Mhz.
- 32Mbyte RAM.
- TCP/IP, NFS, STREAMS.
- 1.2Gbyte of IDE-Hard Drive storage.
- Lynx Operating System version 2.2.

### *SMA1(Submillimeter Array 1(one)):*

Workstation used for scientific and engineering calculations. A gateway(firewall) to the SMA Interferometer and correlator as well as RT imaging.

- Sun 10/40 with a high resolution 20 inch monitor(SPARCstation 10).
- 64Mbytes of Physical Memory(RAM).
- 176Mbytes of Virtual Memory(Swap) .
- 1.2Gbytes of Hard Disk and 3.0Gbyte external SCSI Hard Drive.
- TCP/IP, NFS, OpenWindows Version 3.3.
- SunOS Release 5.3 Generic(Solaris).

### *Soft-RT(Soft Real-Time):*

Minutes, seconds, millisecond responses, as long as the response is deterministic.

### *VME or VMEbus(Versa Module Eurocard or IEEE 1014):*

A crate with a very complex yet easy to understand communications or bus system. Most if not all hardware is plugged into this crate. The CPU can communicate with the hardware via the bus system.

- Each antenna will have a 20 slot VME crate.
- PMACs and other hardware cards will populate the VME crate.
- A VME-MXI extender card will be used to communicate with the VXI crate.

### *VXI or VXIbus(VMEbus Extensions for Instrumentation):*

An extension of the VMEbus system. It has more functionality, better cooled, and better shielded.

- Each antenna will have a 13 slot VXI crate.
- ACCx and DDS cards with will populate the VXI crate
- A VXI-MXI extender card will be used to communicate with the VME crate.

### *Workstation:*

A workstation is a powerful microcomputer typically used for scientific and engineering calculations. A workstation typically has more than 4Mbytes of RAM, more than 100Mbytes of disk capacity, and a screen with graphics resolution of at least 800 X 1000.(D. Downing, M. Covington)

## TABLES for VME backplane and SHRMEM

*All VME data is in 24bit (A24) address space. There is no defined timing to speak of. All the data from the PMAC DPRAM gets mapped as quickly as the PMAC programs run or can update DPRAM which is micro to millisecond times. All SHRMEM data is 32bit address space.*

| ***VME backplane*** | ***SHRMEM*** |
|---|---|
| Address base for ACU, CCU, GCU, YCU, MCU, CU6, CU7, CU8 ..... | |
| • ACU - 0x700000 | 0x0 |
| • CCU - 0x704000 | 0x1000 |
| • GCU - 0x708000 | 0x2000 |
| • YCU - 0x70C000 | 0x3000 |
| • MCU - 0x710000 | 0x4000 |
| • CU6 - 0x714000 | 0x5000 |
| • CU7 - 0x718000 | 0x6000 |
| • CU8 - 0x71C000 | 0x7000 |
| • NON-PMAC - 0x720000 | 0x8000 |
| • CB(Control Building) - 0x724000 | 0x9000 |
| • CV(Control Vault) - 0x728000 | 0xA000 |
| • Tables(Astro. and others) - 0x72C000 | 0xB000 |
| • Spare - 0x730000-7FFFFF | 0xC000 (end of SHRMEM) |
| Address: (Address base + value). | |
| • 0x000-0x7FF:<br>-PMACs own status. | 0x000-0x1FF |
| • 0x800-0xFFF:<br>- Commands.<br>(either RB commands or single shot commands) | 0x200-0x3FF |
| • 0x1000-0x2FFF<br>- Monitor points. | 0x400-0xBFF |
| • 0x3000-0x3FFF<br>- Data gather. | 0xC00-0xFFF |

Robert Calders and I GLOCOM.H include file, Martin Levines notes on the system hardware indentification follow.

```
/* START OF GLOCOM.H */
/*************************************************************************
 *                Smithsonian Astrophysical Observatory                  *
 *                (c) 1993, Submillimeter Array Group                    *
 *                                                                       *
 *                 Include for Shared Memory addressing                  *
 *      This is a common map for all monitor and control points of ACCx  *
 *                                                                       *
 * Version: 1.0  first installation. 12/03/93  (R. Calder, R. Gonzalez)  *
 *                                                                       *
 *************************************************************************/
/*
 * Shared Memory is in compliance with SMA Tech. Memo #75.
 * See memo for more information.
 *
 * If you ever have to get to VME space without going through shared memory
 * remember this: Multiply #define by 4.
 *
 * VME address space is 1byte wide(8bits).
 * Shared Memory space is 4bytes wide(32bits).
 */

/*
 * The first 0x1FF x 32bit values are reserved for the PMACs own status
 * values and ASCII Dual Port RAM communications:
 *
 *      0x0 thru 0x18A   * locations for status values
 *      0x18B thru 0x1F4 * locations for ASCII commands and reponses.
 *
 *      0x1FA             * PMAC to HOST (bit=1) Data Ready.
 *                        * PMAC done updating buffer- Host must clear for more.
 *                        * Servo Timer(Updated at Data Ready Time).
 *      0x1FB            Y* Size of Address Buffer(measured in longs(32bit)).
 *                       X* Start of Address Buffer(Ex. $D400;must be >= $D200).
 *      0x1FC            Y* PMAC to HOST Binary Rotary Buffer Status Word.
 *                       X* Spare.
 *      0x1FD            Y* HOST Binary Rotary buffer index(32bits).
 *                       X* PMAC         "                ( "   ).
 *      0x1FE            Y* Size of Binary Rotary buffer long(32bit).
 *                       X* Starting Binary Rotary buffer PMAC Address(Ex.$D600;
 *                          must be >= $D200.
 *      0x1FF             * Data Gather Buffer Size.
 *                        * PMAC Data Gather Buffer Storage Address.
 *      0x200 thru 0x3FF * locations for rotary buffer commands.
 *      0x400 thru 0xBFF * locations for monitor and control values.
 *      0xC00 thru 0xFFF * locations for data gathering
 */

/*
 * All information will be placed on the VME backplane 0x700000 thru 0x7FFFFF
 * 1MByte x 8bits wide
 */
/*********************************
 * Shared Memory base addresses   *
 *********************************/
#define ACU_SHM_BASE    0x0
#define CCU_SHM_BASE    0x1000
#define GCU_SHM_BASE    0x2000
#define YCU_SHM_BASE    0x3000
#define MCU_SHM_BASE    0x4000
#define CU6_SHM_BASE    0x5000
#define CU7_SHM_BASE    0x6000
#define CU8_SHM_BASE    0x7000
#define NON_SHM_BASE    0x8000
#define CB_SHM_BASE     0x9000
#define CV_SHM_BASE     0xA000
```

```
#define TBL_SHM_BASE    0xB000

/*********************************
 * Shared Memory Map base address *
 *********************************/
#define DP_CMD_BASE     0x18B                   /* Base for Control flag */
#define DP_CNTL_WORD1   DP_CMD_BASE + 0x0       /* command complete */
#define DP_CNTL_WORD2   DP_CMD_BASE + 0x29      /* response ready register */
#define DP_START_INPUT  DP_CMD_BASE + 0x1       /* start of command */
#define DP_NUMOFCHAR    DP_CNTL_WORD2 + 0x0     /* number of char. in response */
#define DP_RESPONSE_BASE        DP_CNTL_WORD2 + 0x1 /* start of response */
#define CMD_BASE        DP_CMD_BASE + 0x75      /* start of rotary commands */
#define DEFINE_BASE     CMD_BASE + 0x201        /* start of monitor data */
#define GATHER_BASE     DEFINE_BASE + 0xC00     /* start of data gathering */

/* Easy to remember address defines */
#define SENDFLAG        0x18B   /* Send Command Control flag */
#define READYFLAG       0x1B4   /* Is response ready flag LS16B */
#define CMDVME          0x18C   /* Start of command */
#define CMDRSVP         0x1B4   /* MS16B # of chars in response */
#define RSVP_CHAR1      0x1B5   /* First char. in response */

/*****************************************
 * Shared Memory PMAC value defines and    *
 * rotary buffer base addresses            *
 *****************************************/
#define ACU_VALUE_BASE  ACU_SHM_BASE + DEFINE_BASE
#define CCU_VALUE_BASE  CCU_SHM_BASE + DEFINE_BASE
#define GCU_VALUE_BASE  GCU_SHM_BASE + DEFINE_BASE
#define YCU_VALUE_BASE  YCU_SHM_BASE + DEFINE_BASE
#define MCU_VALUE_BASE  MCU_SHM_BASE + DEFINE_BASE
#define CU6_VALUE_BASE  CU6_SHM_BASE + DEFINE_BASE
#define CU7_VALUE_BASE  CU7_SHM_BASE + DEFINE_BASE
#define CU8_VALUE_BASE  CU8_SHM_BASE + DEFINE_BASE
#define NON_VALUE_BASE  NON_SHM_BASE + 0x1
#define CB_VALUE_BASE   CB_SHM_BASE + 0x1
#define CV_VALUE_BASE   CV_SHM_BASE + 0x1
#define TBL_VALUE_BASE  TBL_SHM_BASE + 0x1

#define ACU_ROTARY_BASE ACU_SHM_BASE + CMD_BASE
#define CCU_ROTARY_BASE CCU_SHM_BASE + CMD_BASE
#define GCU_ROTARY_BASE GCU_SHM_BASE + CMD_BASE
#define YCU_ROTARY_BASE YCU_SHM_BASE + CMD_BASE
#define MCU_ROTARY_BASE MCU_SHM_BASE + CMD_BASE
#define CU6_ROTARY_BASE CU6_SHM_BASE + CMD_BASE
#define CU7_ROTARY-BASE CU7_SHM_BASE + CMD_BASE
#define CU8_ROTARY_BASE CU8_SHM_BASE + CMD_BASE

/*******************************
 * COMMON                      *
 * Status and servo timer base *
 *******************************/
#define HOST_STAT_PMAC          0x9     /* bit 15 MSB  */
#define DATA_READY_SERVO_TIMER  0x9     /* bits 14-0 LSB */
#define BUFF_STAT_HOSTPMAC      0x8A    /* 16 MSB */
#define PMAC_SERVO_TIMER        0x8A    /* 16 LSB */
#define PMAC_STAT_HOST          0x1FA   /* 16 MSB */
#define DATA_READY_TIMER        0x1FA   /* 16 LSB */
#define BUFF_SIZE               0x1FB   /* 16 MSB */
#define BUFF_START              0x1FB   /* 16 LSB */
#define STATUS_BITS             0x0
#define INDEX                   0x1

/**************
 * Motor base *
 **************/
```

```
#define MOTOR1                  ACU_SHM_BASE + 0x12
#define MOTOR2                  MOTOR1 + 0xF
#define MOTOR3                  MOTOR2 + 0xF
#define MOTOR4                  MOTOR3 + 0xF
#define MOTOR5                  MOTOR4 + 0xF
#define MOTOR6                  MOTOR5 + 0xF
#define MOTOR7                  MOTOR6 + 0xF
#define MOTOR8                  MOTOR7 + 0xF
#define MOTOR1_CS               ACU_SHM_BASE + 0x93
#define MOTOR2_CS               MOTOR1 + 0x1F
#define MOTOR3_CS               MOTOR2 + 0x1F
#define MOTOR4_CS               MOTOR3 + 0x1F
#define MOTOR5_CS               MOTOR4 + 0x1F
#define MOTOR6_CS               MOTOR5 + 0x1F
#define MOTOR7_CS               MOTOR6 + 0x1F
#define MOTOR8_CS               MOTOR7 + 0x1F

/*******************
 * Motor indexes   *
 * MOTORx + define *
 *******************/
#define A_CMD_POS               0x0
#define A_ACTUAL_POS            0x2
#define A_MASTER_POS            0x4
#define A_COMPENS_POS           0x6
#define A_PREVIOUS_DAC          0x8
#define A_SERVO_STATUS          0x9
#define A_ACTUAL_VEL            0xA
#define A_TIME_LEFT             0xB
#define A_SPARE                 0xC

/************************************
 * Motor and Corr. Systems indexes  *
 * MOTORx_CS + define               *
 ************************************/
#define A_CS_TARPOS                     0x0
#define A_CS_POS_BAIS                   0x2
#define A_CS_MOTOR_STATUS_WORD          0x4
#define A_CS_STATUS_DEFINE_WORD         0x5
#define A_CS_AAXIS_TARPOS               0x7
#define A_CS_BAXIS_TARPOS               0x9
#define A_CS_CAXIS_TARPOS               0xB
#define A_CS_UAXIS_TARPOS               0xD
#define A_CS_VAXIS_TARPOS               0xF
#define A_CS_WAXIS_TARPOS               0x11
#define A_CS_XAXIS_TARPOS               0x13
#define A_CS_YAXIS_TARPOS               0x15
#define A_CS_ZAXIS_TARPOS               0x17
#define A_CS_PROG_EXEC_STATUS           0x19
#define A_CS_PROG_LINES_REMAIN          0x1A
#define A_CS_MOVE_TIME_REMAIN           0x1B
#define A_CS_ACCEL_DECEL_TIME_REMAIN    0x1C
#define A_CS_PROG_EXEC_ADDR_OFFSET      0x1D
#define A_CS_SPARE                      0x1E

/*********************************************************
 * ACU                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x701004 thru 0x703FFF                      *
 * Stored in Shared Memory 0x401 thru 0xFFF              *
 *********************************************************/
#define A_HOST_PMAC_STATUS      ACU_SHM_BASE + HOST_PMAC_STATUS
#define A_BUFF_STAT_HOSTPMAC    ACU_SHM_BASE + BUFF_STAT_HOSTPMAC
#define A_PMAC_SERVO_TIMER      ACU_SHM_BASE + PMAC_SERVO_TIMER
#define A_M1                    0x0
```

```
#define A_M2                    A_M1 + 0x12
#define A_M3                    A_M2 + 0x12
#define A_M4                    A_M3 + 0x12
#define A_M5                    A_M4 + 0x12
#define A_M6                    A_M5 + 0x12
#define A_M7                    A_M6 + 0x12
#define A_M8                    A_M7 + 0x12
#define A_CS1                   0x0
#define A_CS2                   A_CS1 + 0x0
#define A_CS3                   A_CS2 + 0x0
#define A_CS4                   A_CS3 + 0x0
#define A_CS5                   A_CS4 + 0x0
#define A_CS6                   A_CS5 + 0x0
#define A_CS7                   A_CS6 + 0x0
#define A_CS8                   A_CS7 + 0x0

/* Status bits are as follows
 * None
 */
#define A_STATUS_BITS           ACU_VALUE_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

#define A_PRESENT_AZ_POS        ACU_VALUE_BASE + 0x1
#define A_PRESENT_AZ_VEL        ACU_VALUE_BASE + 0x2
#define A_PRESENT_AZ_FOL        ACU_VALUE_BASE + 0x3
#define A_CMDED_AZ_POS          ACU_VALUE_BASE + 0x4
#define A_PRESENT_EL_POS        ACU_VALUE_BASE + 0x5
#define A_PRESENT_EL_VEL        ACU_VALUE_BASE + 0x6
#define A_PRESENT_EL_FOL        ACU_VALUE_BASE + 0x7
#define A_CMDED_EL_POS          ACU_VALUE_BASE + 0x8
#define A_AZ_MOTOR1_CURRENT     ACU_VALUE_BASE + 0x9
#define A_AZ_MOTOR2_CURRENT     ACU_VALUE_BASE + 0xA
#define A_EL_MOTOR_CURRENT      ACU_VALUE_BASE + 0xB
#define A_ANT_STATUS1           ACU_VALUE_BASE + 0xC
#define A_ANT_STATUS2           ACU_VALUE_BASE + 0xD
#define A_TILT1                 ACU_VALUE_BASE + 0xE
#define A_TILT2                 ACU_VALUE_BASE + 0xF
#define A_TILT3                 ACU_VALUE_BASE + 0x10
#define A_MUX_ANT_STRUCT_TEMP   ACU_VALUE_BASE + 0x11

/*********************************************************
 * CCU                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x705004 thru 0x707FFF                      *
 * Stored in Shared Memory 0x1401 thru 0x1FFF            *
 *********************************************************/
#define C_HOST_PMAC_STATUS      CCU_SHM_BASE + HOST_PMAC_STATUS
#define C_HOST_STAT_PMAC        CCU_SHM_BASE + HOST_STAT_PMAC
#define C_BUFF_STAT_HOSTPMAC    CCU_SHM_BASE + BUFF_STAT_HOSTPMAC
#define C_PMAC_SERVO_TIMER      CCU_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
 * None
 */
#define C_STATUS_BITS           CCU_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */
```

```
#define C_POS           CCU_VALUE_BASE + 0x1
#define C_FOL           CCU_VALUE_BASE + 0x2
#define C_XPOS          CCU_VALUE_BASE + 0x3
#define C_YPOS          CCU_VALUE_BASE + 0x4
#define C_ZPOS          CCU_VALUE_BASE + 0x5


/*********************************************************
 * GCU                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x709004 thru 0x70BFFF                      *
 * Stored in Shared Memory 0x2401 thru 0x2FFF            *
 *********************************************************/
#define G_HOST_PMAC_STATUS      GCU_SHM_BASE + HOST_PMAC_STATUS
#define G_HOST_STAT_PMAC        GCU_SHM_BASE + HOST_STAT_PMAC
#define G_BUFF_STAT_HOSTPMAC    GCU_SHM_BASE + BUFF_STAT_HOSTPMAC
#define G_PMAC_SERVO_TIMER      GCU_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
 *      HW                              bit
 * G_DISABLEA                            0 *Gunn oscillator monitor/control
 * G_FAULTA                              1      "
 * G_DISABLEB                            2      "
 * G_FAULTB                              3      "
 * G_PLL_DIABLEA                         4 *Gunn oscillator phaselock servo
 * G_PLL_DIABLEB                         5      "
 */
#define G_STATUS_BITS           GCU_SHM_BASE + STATUS_BITS
/*
 *       31         21         11         0
 * bits  |          |          |          |
 *       01234567890123456789012345678901
 */

/* GUNN oscillator monitor/control */
#define G_OSC_SELECTA_CMD       GCU_VALUE_BASE + 0x1
#define G_VOLTAGEA              GCU_VALUE_BASE + 0x2
#define G_CURRENTA              GCU_VALUE_BASE + 0x3
#define G_OSC_SELECTB_CMD       GCU_VALUE_BASE + 0x4
#define G_VOLTAGEB              GCU_VALUE_BASE + 0x5
#define G_CURRENTB              GCU_VALUE_BASE + 0x6

/* GUNN oscillator phaselock servo */
#define G_FINE_TUNEA_CMD        GCU_VALUE_BASE + 0x7
#define G_MAIN_TUNEA_CMD        GCU_VALUE_BASE + 0x8
#define G_BACKSHORTA_CMD        GCU_VALUE_BASE + 0x9
#define G_IF_GAINLOA_CMD        GCU_VALUE_BASE + 0xA
#define G_IF_GAINHIA_CMD        GCU_VALUE_BASE + 0xB
#define G_PLL_ERRORA            GCU_VALUE_BASE + 0xC
#define G_LOCKA                 GCU_VALUE_BASE + 0xD
#define G_FINE_TUNEB_CMD        GCU_VALUE_BASE + 0xE
#define G_MAIN_TUNEB_CMD        GCU_VALUE_BASE + 0xF
#define G_BACKSHORTB_CMD        GCU_VALUE_BASE + 0x10
#define G_IF_GAINLOB_CMD        GCU_VALUE_BASE + 0x11
#define G_IF_GAINHIB_CMD        GCU_VALUE_BASE + 0x12
#define G_PLL_ERRORB            GCU_VALUE_BASE + 0x13
#define G_LOCKB                 GCU_VALUE_BASE + 0x14

/* GUNN DDS monitor/control */
#define G_DDS_FREQA_CMD         GCU_VALUE_BASE + 0x15
#define G_DDS_PHASEA_CMD        GCU_VALUE_BASE + 0x16
#define G_DDS_FMA_CMD           GCU_VALUE_BASE + 0x17
#define G_DDS_LEVELA            GCU_VALUE_BASE + 0x18
#define G_DDS_FREQB_CMD         GCU_VALUE_BASE + 0x19
#define G_DDS_PHASEB_CMD        GCU_VALUE_BASE + 0x1A
```

```
#define G_DDS_FMB_CMD           GCU_VALUE_BASE + 0x1B
#define G_DDS_LEVELB            GCU_VALUE_BASE + 0x1C

/* Harmonic mixer monitor/control */
#define G_HARM_MIXER_IF_SW_CMD          GCU_VALUE_BASE + 0x1D
#define G_HARM_MIXER_REF_SW_CMD         GCU_VALUE_BASE + 0x1E
#define G_HARM_MIXER_BIAS_SW_CMD        GCU_VALUE_BASE + 0x1F

/*********************************************************
 * YCU                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x70D004 thru 0x70FFFF                      *
 * Stored in Shared Memory 0x3401 thru 0x3FFF            *
 *********************************************************/
#define Y_HOST_PMAC_STATUS      YCU_SHM_BASE + HOST_PMAC_STATUS
#define Y_HOST_STAT_PMAC        YCU_SHM_BASE + HOST_STAT_PMAC
#define Y_BUFF_STAT_HOSTPMAC    YCU_SHM_BASE + BUFF_STAT_HOSTPMAC
#define Y_PMAC_SERVO_TIMER      YCU_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
        HW                          bit
 * Y_PLL_DISABLEA                    0  *Ref. signal generator phaselock servo
 * Y_PLL_DISABLEB                    1             "
 * Y_PS_DISABLEA                     2  *Ref. signal generator PS monito/control
 * Y_PS_FAULTA                       3             "
 * Y_PS_DISABLEB                     4             "
 * Y_PS_FAULTB                       5             "
 * Y_MAIN_PS_18V_FAULT     6  *Main power supply monitor/control
 * Y_MAIN_PS_N18V_FAULT              7             "
 * Y_MAIN_PS_N8V_FAULT               8             "
 * Y_MAIN_PS_18V_DISABLE             9             "
 * Y_MAIN_PS_N18V_DISABLE           10             "
 * Y_MAIN_PS_+8V_DISABLE            11             "
 */
#define Y_STATUS_BITS           YCU_SHM_BASE + STATUS_BITS
/*
 *       31         21         11          0
 * bits  |          |          |          |
 *       01234567890123456789012345678901
 */

/* Fiber Optics Receiver M/C */
#define Y_FO_REC_LEVELA YCU_VALUE_BASE + 0x1
#define Y_FO_RCVR_TEMPA YCU_VALUE_BASE + 0x2
#define Y_FO_RCVR_HTR_PWRA      YCU_VALUE_BASE + 0x3
#define Y_FO_REC_LEVELB YCU_VALUE_BASE + 0x4
#define Y_FO_RCVR_TEMPB YCU_VALUE_BASE + 0x5
#define Y_FO_RCVR_HTR_PWRB      YCU_VALUE_BASE + 0x6

/* Reference Signal Generator Phase Lock Servo */
#define Y_TUNINGA_CMD           YCU_VALUE_BASE + 0x7
#define Y_IF_GAINA_CMD          YCU_VALUE_BASE + 0x8
#define Y_LOCKA         YCU_VALUE_BASE + 0x9
#define Y_FM_TUNINGA            YCU_VALUE_BASE + 0xA
#define Y_MAIN_TUNINGA          YCU_VALUE_BASE + 0xB
#define Y_TUNINGB_CMD           YCU_VALUE_BASE + 0xC
#define Y_IF_GAINB_CMD          YCU_VALUE_BASE + 0xD
#define Y_LOCKB         YCU_VALUE_BASE + 0xE
#define Y_FM_TUNINGB            YCU_VALUE_BASE + 0xF
#define Y_MAIN_TUNINGB          YCU_VALUE_BASE + 0x10

/* RSG ALC M/C */
#define Y_ALC_LEVELA_CMD        YCU_VALUE_BASE + 0x11
#define Y_ALC_SIGNAL_LEVELA     YCU_VALUE_BASE + 0x12
#define Y_ATTEN_LEVELA          YCU_VALUE_BASE + 0x13
```

```
#define Y_ALC_LEVELB_CMD        YCU_VALUE_BASE + 0x14
#define Y_ALC_SIGNAL_LEVELB     YCU_VALUE_BASE + 0x15
#define Y_ATTEN_LEVELB          YCU_VALUE_BASE + 0x16

/* RSG Frequency Synthesizer M/C */
#define Y_FREQ_SYN2_LEVELA      YCU_VALUE_BASE + 0x17
#define Y_FREQ_SYN2_LOCKA       YCU_VALUE_BASE + 0x18
#define Y_FREQ_SYN2_TUNEA_CMD   YCU_VALUE_BASE + 0x19
#define Y_FREQ_SYN2_LEVELB      YCU_VALUE_BASE + 0x1A
#define Y_FREQ_SYN2_LOCKB       YCU_VALUE_BASE + 0x1B
#define Y_FREQ_SYN2_TUNEB_CMD   YCU_VALUE_BASE + 0x1C

/* Main power supply monitor/control */
#define Y_MAIN_PS_18V           YCU_VALUE_BASE + 0x1D
#define Y_MAIN_PS_18I           YCU_VALUE_BASE + 0x1E
#define Y_MAIN_PS_N18V          YCU_VALUE_BASE + 0x1F
#define Y_MAIN_PS_N18I          YCU_VALUE_BASE + 0x20
#define Y_MAIN_PS_8V            YCU_VALUE_BASE + 0x21
#define Y_MAIN_PS_N8I           YCU_VALUE_BASE + 0x22

/*********************************************************
 * MCU                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x711004 thru 0x713FFF                      *
 * Stored in Shared Memory 0x4401 thru 0x4FFF            *
 *********************************************************/
#define M_HOST_PMAC_STATUS      MCU_SHM_BASE + HOST_PMAC_STATUS
#define M_HOST_STAT_PMAC        MCU_SHM_BASE + HOST_STAT_PMAC
#define M_BUFF_STAT_HOSTPMAC    MCU_SHM_BASE + BUFF_STAT_HOSTPMAC
#define M_PMAC_SERVO_TIMER      MCU_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
 * None
 */
#define M_STATUS_BITS           MCU_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

#define M_MULT1_BS_POS_MON      MCU_VALUE_BASE + 0x1
#define M_MULT1_BS_POS_CMD      MCU_VALUE_BASE + 0x2
#define M_MULT1_TUNE_POS_MON    MCU_VALUE_BASE + 0x3
#define M_MULT1_TUNE_POS_CMD    MCU_VALUE_BASE + 0x4
#define M_MULT2_BS_POS_MON      MCU_VALUE_BASE + 0x5
#define M_MULT2_BS_POS_CMD      MCU_VALUE_BASE + 0x6
#define M_MULT2_TUNE_POS_MON    MCU_VALUE_BASE + 0x7
#define M_MULT2_TUNE_POS_CMD    MCU_VALUE_BASE + 0x8
#define M_MULT3_BS_POS_MON      MCU_VALUE_BASE + 0x9
#define M_MULT3_BS_POS_CMD      MCU_VALUE_BASE + 0xA
#define M_MULT3_TUNE_POS_MON    MCU_VALUE_BASE + 0xB
#define M_MULT3_TUNE_POS_CMD    MCU_VALUE_BASE + 0xC
#define M_MULT4_BS_POS_MON      MCU_VALUE_BASE + 0xD
#define M_MULT4_BS_POS_CMD      MCU_VALUE_BASE + 0xE
#define M_MULT4_TUNE_POS_MON    MCU_VALUE_BASE + 0xF
#define M_MULT4_TUNE_POS_CMD    MCU_VALUE_BASE + 0x10

/*********************************************************
 * CU6                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x715004 thru 0x717FFF                      *
 * Stored in Shared Memory 0x5401 thru 0x5FFF            *
 *********************************************************/
```

```
#define CU6_HOST_PMAC_STATUS    CU6_SHM_BASE + HOST_PMAC_STATUS
#define CU6_HOST_STAT_PMAC      CU6_SHM_BASE + HOST_STAT_PMAC
#define CU6_BUFF_STAT_HOSTPMAC  CU6_SHM_BASE + BUFF_STAT_HOSTPMAC
#define CU6_PMAC_SERVO_TIMER    CU6_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
 * None
 */
#define CU6_STATUS_BITS         CU6_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

/*********************************************************
 * CU7                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x719004 thru 0x71BFFF                      *
 * Stored in Shared Memory 0x6401 thru 0x6FFF            *
 *********************************************************/
#define CU7_HOST_PMAC_STATUS    CU7_SHM_BASE + HOST_PMAC_STATUS
#define CU7_HOST_STAT_PMAC      CU7_SHM_BASE + HOST_STAT_PMAC
#define CU7_BUFF_STAT_HOSTPMAC  CU7_SHM_BASE + BUFF_STAT_HOSTPMAC
#define CU7_PMAC_SERVO_TIMER    CU7_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
 * None
 */
#define CU7_STATUS_BITS         CU7_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

/*********************************************************
 * CU8                                                   *
 * Monitor and Control data from PMAC                    *
 * DPRAM $D401 - $DFFF                                   *
 * VME space 0x71D004 thru 0x71FFFF                      *
 * Stored in Shared Memory 0x7401 thru 0x7FFF            *
 *********************************************************/
#define CU8_HOST_PMAC_STATUS    CU8_SHM_BASE + HOST_PMAC_STATUS
#define CU8_HOST_STAT_PMAC      CU8_SHM_BASE + HOST_STAT_PMAC
#define CU8_BUFF_STAT_HOSTPMAC  CU8_SHM_BASE + BUFF_STAT_HOSTPMAC
#define CU8_PMAC_SERVO_TIMER    CU8_SHM_BASE + PMAC_SERVO_TIMER

/* Status bits are as follows
 * None
 */
#define CU8_STATUS_BITS         CU8_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

/*********************************************************
 * NON-PMAC                                              *
 * VME space 0x720004 thru 0x723FFFF                     *
 * Stored in Shared Memory 0x8001 thru 0x8FFF            *
 *********************************************************/
/* Status bits are as follows
 *      HW                      bits
```

```
 * NON_FO_XMTR_MODA              0       *Laser transmitter monitor/control
 * NON_FO_XMTR_OVRTMPA           1               "
 * NON_FO_XMTR_DISABLEA  2               "
 * NON_FO_XMTR_SHUTTERA  3               "
 * NON_FO_XMTR_MODB              4               "
 * NON_FO_XMTR_OVRTMPB           5               "
 * NON_FO_XMTR_DISABLEB  6               "
 * NON_FO_XMTR_SHUTTERB  7               "
 * NON_MAIN_PS_18V_FAULT         8  *Main power supply monitor/control
 * NON_MAIN_PS_N18V_FAULT        9       "
 * NON_MAIN_PS_8V_FAULT          10      "
 * NON_MAIN_PS_18V_DISABLE       11      "
 * NON_MAIN_PS_N18V_DISABLE      12      "
 * NON_MAIN_PS_8V_DISABLE        13      "
 */
#define NON_STATUS_BITS          NON_SHM_BASE + STATUS_BITS
/*
 *       31         21         11          0
 * bits  |          |          |          |
 *       01234567890123456789012345678901
 */

/* Laser transmitter monitor/control */
#define NON_FO_XMTR_TEMPA        NON_VALUE_BASE + 0x1
#define NON_FO_XMTR_HTR_PWRA     NON_VALUE_BASE + 0x2
#define NON_FO_XMTR_OPT_MONA     NON_VALUE_BASE + 0x3
#define NON_FO_XMTR_LASERA       NON_VALUE_BASE + 0x4
#define NON_FO_XMTR_THERMALA     NON_VALUE_BASE + 0x5
#define NON_FO_XMTR_TEMPB        NON_VALUE_BASE + 0x6
#define NON_FO_XMTR_HTR_PWRB     NON_VALUE_BASE + 0x7
#define NON_FO_XMTR_OPT_MONB     NON_VALUE_BASE + 0x8
#define NON_FO_XMTR_LASERB       NON_VALUE_BASE + 0x9
#define NON_FO_XMTR_THERMALB     NON_VALUE_BASE + 0xA

/* TotalPower Detector monitor/control */
#define NON_TDC_CONTR_LEVELA     NON_VALUE_BASE + 0xB
#define NON_TDC_MEAS_LEVELA      NON_VALUE_BASE + 0xC
#define NON_TDC_TEMPA    NON_VALUE_BASE + 0xD
#define NON_TDC_HTR_PWRA         NON_VALUE_BASE + 0xE
#define NON_TDC_CONTR_LEVELB     NON_VALUE_BASE + 0xF
#define NON_TDC_MEAS_LEVELB      NON_VALUE_BASE + 0x10
#define NON_TDC_TEMPB    NON_VALUE_BASE + 0x11
#define NON_TDC_HTR_PWRB         NON_VALUE_BASE + 0x12

/* Receiver ALC monitor/control */
#define NON_ALC_LEVEL_SETA_CMD           NON_VALUE_BASE + 0x13
#define NON_ALC_SIGNAL_LEVELA            NON_VALUE_BASE + 0x14
#define NON_ALC_ATTEN_LEVELA             NON_VALUE_BASE + 0x15
#define NON_ALC_LEVEL_SETB_CMD           NON_VALUE_BASE + 0x16
#define NON_ALC_SIGNAL_LEVELB            NON_VALUE_BASE + 0x17
#define NON_ALC_ATTEN_LEVELB             NON_VALUE_BASE + 0x18

/* Digital attenuator monitor/control */
#define NON_DIGITAL_ATTEN_SETA_CMD       NON_VALUE_BASE + 0x19
#define NON_DIGITAL_ATTEN_SETB_CMD       NON_VALUE_BASE + 0x1A

/* Main power supply monitor/control */
#define NON_MAIN_PS_18V          NON_VALUE_BASE + 0x1B
#define NON_MAIN_PS_18I          NON_VALUE_BASE + 0x1C
#define NON_MAIN_PS_N18V         NON_VALUE_BASE + 0x1D
#define NON_MAIN_PS_N18I                 NON_VALUE_BASE + 0x1E
#define NON_MAIN_PS_8V           NON_VALUE_BASE + 0x1F
#define NON_MAIN_PS_N8I          NON_VALUE_BASE + 0x20

/*****************************************************
 * CONTROL BUILDING                                  *
```

```
 * VME space 0x724004 thru 0x727FFFF                          *
 * Stored in Shared Memory 0x9001 thru 0x9FFF                 *
 ************************************************************/
/* Status bits are as follows
 *      HW                          bits
 * CB_MAIN_PS_18V_FAULT             0  *Main power supply monitor/control
 * CB_MAIN_PS_N18V_FAULT            1      "
 * CB_MAIN_PS_8V_FAULT              2      "
 * CB_MAIN_PS_18V_DISABLE           3      "
 * CB_MAIN_PS_N18V_DISABLE          4      "
 * CB_MAIN_PS_N8V_DISABLE           5      "
 */
#define CB_STATUS_BITS          CB_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

/* Fiberoptic RCVR monitor/control */
#define CB_FO_REC_LEVELA        CB_VALUE_BASE + 0x1
#define CB_FO_RCVR_TEMPA        CB_VALUE_BASE + 0x2
#define CB_FO_RCVR_HTR_PWRA     CB_VALUE_BASE + 0x3
#define CB_FO_REC_LEVELB        CB_VALUE_BASE + 0x4
#define CB_FO_RCVR_TEMPB        CB_VALUE_BASE + 0x5
#define CB_FO_RCVR_HTR_PWRB     CB_VALUE_BASE + 0x6

/* Receiver ALC monitor/control */
#define CB_ALC_LEVEL_SETA_CMD   CB_VALUE_BASE + 0x7
#define CB_ALC_SIGNAL_LEVELA    CB_VALUE_BASE + 0x8
#define CB_ALC_ATTEN_LEVELA     CB_VALUE_BASE + 0x9
#define CB_ALC_LEVEL_SETB_CMD   CB_VALUE_BASE + 0xA
#define CB_ALC_SIGNAL_LEVELB    CB_VALUE_BASE + 0xB
#define CB_ALC_ATTEN_LEVELB     CB_VALUE_BASE + 0xC

/* Digital attenuator monitor/control */
#define CB_DIGITAL_ATTEN_SETA_CMD       CB_VALUE_BASE + 0xD
#define CB_DIGITAL_ATTEN_SETB_CMD       CB_VALUE_BASE + 0xE

/* Main power supply monitor/control */
#define CB_MAIN_PS_18V          CB_VALUE_BASE + 0xF
#define CB_MAIN_PS_18I          CB_VALUE_BASE + 0x10
#define CB_MAIN_PS_N18V         CB_VALUE_BASE + 0x11
#define CB_MAIN_PS_N18I         CB_VALUE_BASE + 0x12
#define CB_MAIN_PS_8V           CB_VALUE_BASE + 0x13
#define CB_MAIN_PS_N8I          CB_VALUE_BASE + 0x14

/************************************************************
 * CENTRAL VAULT                                            *
 * VME space 0x728004 thru 0x72BFFFF                        *
 * Stored in Shared Memory 0xA001 thru 0xAFFF               *
 ************************************************************/
/* Status bits are as follows
 *      HW                          bits
 * CV_10MHz_SWEEP                   0      *10MHz phaselock servo
 * CV_100MHz_SWEEP                  1      *100MHz phaselock servo
 * CV_YIG_PLL_DISABLEA              2      *Master ref. generator Phaselock servo
 * CV_YIG_PLL_DISABLEB              3      *Master ref. generator Phaselock servo
 * CV_PS_DISABLEA                   4      *Master ref. generator PS mon/con
 * CV_PS_FAULTA                     5             "
 * CV_PS_DISABLEB                   6             "
 * CV_PS_FAULTB          7                "
 * CV_FO_XMTR_MODA                  8      *Laser transmitter monitor/control
 * CV_FO_XMTR_OVRTMPA               9             "
 * CV_FO_XMTR_DISABLEA              10            "
 * CV_FO_XMTR_SHUTTERA              11            "
```

```
 * CV_FO_XMTR_MODB                12              "
 * CV_FO_XMTR_OVRTMPB             13              "
 * CV_FO_XMTR_DISABLEB            14              "
 * CV_FO_XMTR_SHUTTERB            15              "
 * CV_MAIN_PS_18V_FAULT           16      *Main power supply monitor/control
 * CV_MAIN_PS_N18V_FAULT          17              "
 * CV_MAIN_PS_8V_FAULT            18              "
 * CV_MAIN_PS_18V_DISABLE         19              "
 * CV_MAIN_PS_N18V_DISABLE        20              "
 * CV_MAIN_PS_8V_DISABLE          21              "
 */
#define CV_STATUS_BITS          CV_SHM_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

/* 10MHz generator monitor/control */
#define CV_10MHZ_LEVEL  CV_VALUE_BASE + 0x1

/* 10MHz phaselock servo */
#define CV_10MHZ_LOCK                   CV_VALUE_BASE + 0x2
#define CV_10MHZ_FINE_TUNING_CMD        CV_VALUE_BASE + 0x3

/* 1.0GHz generator monitor/control */
#define CV_1GHZ_LEVEL   CV_VALUE_BASE + 0x4

/* 6 GHz generator monitor/control */
#define CV_BAND_SELECT  CV_VALUE_BASE + 0x5
#define CV_6GHZ_LEVEL   CV_VALUE_BASE + 0x6

/* Master ref. generator phaselock servo */
#define CV_YIG_TUNINGA_CMD      CV_VALUE_BASE + 0x7
#define CV_YIG_IF_GAINA_CMD     CV_VALUE_BASE + 0x8
#define CV_YIG_LOCKA            CV_VALUE_BASE + 0x9
#define CV_YIG_FM_TUNINGA       CV_VALUE_BASE + 0xA
#define CV_YIG_MAIN_TUNINGA     CV_VALUE_BASE + 0xB
#define CV_YIG_TUNINGB_CMD      CV_VALUE_BASE + 0xC
#define CV_YIG_IF_GAINB_CMD     CV_VALUE_BASE + 0xD
#define CV_YIG_LOCKB            CV_VALUE_BASE + 0xE
#define CV_YIG_FM_TUNINGB       CV_VALUE_BASE + 0xF
#define CV_YIG_MAIN_TUNINGB     CV_VALUE_BASE + 0x10

/* MRG freq. synthesizer monitor/control */
#define CV_FREQ_SYN1A           CV_VALUE_BASE + 0x11
#define CV_FREQ_SYN1B           CV_VALUE_BASE + 0x12

/* MRG ALC M/C */
#define CV_YIG_ALC_LEVELA_CMD           CV_VALUE_BASE + 0x13
#define CV_YIG_ALC_SIGNAL_LEVELA        CV_VALUE_BASE + 0x14
#define CV_YIG_ATTEN_LEVELA             CV_VALUE_BASE + 0x15
#define CV_YIG_ALC_LEVELB_CMD           CV_VALUE_BASE + 0x16
#define CV_YIG_ALC_SIGNAL_LEVELB        CV_VALUE_BASE + 0x17
#define CV_YIG_ATTEN_LEVELB             CV_VALUE_BASE + 0x18

/* Laser transmitter monitor/control */
#define CV_FO_XMTR_TEMPA        CV_VALUE_BASE + 0x19
#define CV_FO_XMTR_HTR_PWRA     CV_VALUE_BASE + 0x1A
#define CV_FO_XMTR_OPT_MONA     CV_VALUE_BASE + 0x1B
#define CV_FO_XMTR_LASERA       CV_VALUE_BASE + 0x1C
#define CV_FO_XMTR_THERMALA     CV_VALUE_BASE + 0x1D
#define CV_FO_XMTR_TEMPB        CV_VALUE_BASE + 0x1E
#define CV_FO_XMTR_HTR_PWRB     CV_VALUE_BASE + 0x1F
#define CV_FO_XMTR_OPT_MONB     CV_VALUE_BASE + 0x20
#define CV_FO_XMTR_LASERB       CV_VALUE_BASE + 0x21
```

```
#define CV_FO_XMTR_THERMALB     CV_VALUE_BASE + 0x22

/* Main power supply monitor/control */
#define CV_MAIN_PS_18V          CV_VALUE_BASE + 0x23
#define CV_MAIN_PS_18I          CV_VALUE_BASE + 0x24
#define CV_MAIN_PS_N18V         CV_VALUE_BASE + 0x25
#define CV_MAIN_PS_N18I         CV_VALUE_BASE + 0x26
#define CV_MAIN_PS_8V           CV_VALUE_BASE + 0x27
#define CV_MAIN_PS_N8I          CV_VALUE_BASE + 0x28


/*********************************************************
 * Astronamical, LO/IF, and misc. TABLES                 *
 * VME space 0x72D004 thru 0x72FFFF                      *
 * Stored in Shared Memory 0xB001 thru 0xBFFF            *
 *********************************************************/

/* Status bits are as follows
 * None
 */
#define TBL_STATUS_BITS         TBL_VALUE_BASE + STATUS_BITS
/*
 *       31        21        11         0
 * bits  |         |         |         |
 *       01234567890123456789012345678901
 */

/* END OF GLOCOM.H */
```

## CENTRAL VAULT REFERENCE SIGNAL FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| 10 MHz GENERATOR CONTROL/MONITOR | | | | | | | |
| 10 MHz LEVEL | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| 10 MHz PHASELOCK SERVO | | | | | | | |
| 10 MHz LOCK | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| 10 MHz SWEEP | CONTROL | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | | 0.01 SECOND |
| 10 MHz FINE TUNING | CONTROL | ANALOG | 12 BIT | TIME SENSITIVE | TRIGGERED | TURN-ON | 0.01 SECOND |
| 100 MHz GENERATOR CONTROL/MONITOR | | | | | | | |
| 100 MHz LEVEL | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| 100 MHz PHASELOCK SERVO | | | | | | | |
| 100 MHz LOCK | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| 100 MHz SWEEP | CONTROL | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | | 0.01 SECOND |
| 100 MHz FINE TUNING | CONTROL | ANALOG | 12 BIT | TIME SENSITIVE | TRIGGERED | TURN-ON | 0.01 SECOND |
| 1.0 GHz GENERATOR CONTROL/MONITOR | | | | | | | |
| 1.0 GHz LEVEL | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| 6 GHz GENERATOR CONTROL/MONITOR | | | | | | | |
| BAND SELECT | CONTROL | NONE | 2 BIT | RELAY DRIVER | TRIGGERED | SET-UP | ONE-TIME |
| 6 GHz LEVEL | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | |
| MASTER REFERENCE GENERATOR PHASELOCK SERVO | | | | | | | |
| YIG TUNING- A | CONTROL | ANALOG | 16 BIT | TIME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG IF GAIN- A | CONTROL | ANALOG | 8-BIT EQUIV | TME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG PLL DISABLE- A | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | CALIBRATION | 0.01 SECOND |
| YIG LOCK- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG FM TUNING- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG MAIN TUNING- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG TUNING- B | CONTROL | ANALOG | 16 BIT | TIME SENSITIVE | TRIGGERED | CALIBRATION | 0.01 SECOND |
| YIG IF GAIN- B | CONTROL | ANALOG | 8-BIT EQUIV | TME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG PLL DISABLE- B | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | CALIBRATION | 0.01 SECOND |
| YIG LOCK- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG FM TUNING- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG MAIN TUNING- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |

## CENTRAL VAULT REFERENCE SIGNAL FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| MASTER REFERENCE GENERATOR PS CONTROL/MONITOR | | | | | | | |
| YIG PS DISABLE- A | CONTROL | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.1 SECOND |
| YIG PS FAULT- A | FLAG | ON/OFF | N/A | TIME SENSITIVE | CONTINUOUS | | 0.1 SECOND |
| YIG PS DISABLE- B | CONTROL | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.1 SECOND |
| YIG PS FAULT- B | FLAG | ON/OFF | N/A | TIME SENSITIVE | CONTINUOUS | | 0.1 SECOND |
| MRG FREQ SYNTHESIZER CONTROL/MONITOR | | | | | | | |
| FREQ SYN1- A | CONTROL | IEEE-488 | STANDARD | | TRIGGERED | SET-UP | 0.1 SECOND |
| FREQ SYN1- B | CONTROL | IEEE-488 | STANDARD | | TRIGGERED | SET-UP | 0.1 SECOND |
| MRG ALC CONTROL/MONITOR | | | | | | | |
| ALC LEVEL SET- A | CONTROL | ANALOG | 8 BIT | | TRIGGERED | CALIBRATION | 0.1 SECOND |
| ALC SIGNAL LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC LEVEL SET- B | CONTROL | ANALOG | 8 BIT | | TRIGGERED | CALIBRATION | 0.1 SECOND |
| ALC SIGNAL LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| LASER TRANSMITTER CONTROL/MONITOR | | | | | | | |
| FO XMTR TEMP- A | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO XMTR HTR PWR- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR OPT MON- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR LASER- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR THERMAL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR MOD- A | GATE | ON/OFF | N/A | TIME SENSITIVE SAFE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR OVRTMP- A | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR DISABLE- A | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR SHUTTER- A | GATE | ON/OFF | N/A | TIME SENSITIVE SAFE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR TEMP- B | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO XMTR HTR PWR- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR OPT MON- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR LASER- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR THERMAL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR MOD- B | GATE | ON/OFF | N/A | TIME SENSITIVE SAFE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR OVRTMP- B | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR DISABLE- B | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR SHUTTER- B | GATE | ON/OFF | N/A | TIME SENSITIVE SAFE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN POWER SUPPLY CONTROL/MONITOR | | | | | | | |

## CENTRAL VAULT REFERENCE SIGNAL FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| MAIN PS +18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |

## ANTENNA REFERENCE SIGNAL SOFTWARE FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| FIBEROPTIC RCVR CONTROL/MONITOR | | | | | | | |
| FO REC LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO RCVR TEMP- A | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO RCVR HTR PWR- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO REC LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO RCVR TEMP- B | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO RCVR HTR PWR- | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| REFERENCE SIGNAL GENERATOR PHASELOCK SERVO | | | | | | | |
| YIG TUNING- A | CONTROL | ANALOG | 16 BIT | TIME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG IF GAIN- A | CONTROL | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG PLL DISABLE- A | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | | 0.01 SECOND |
| YIG LOCK- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG FM TUNING- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG MAIN TUNING- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG TUNING- B | CONTROL | ANALOG | 16 BIT | TIME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG IF GAIN- B | CONTROL | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | PERIODIC | CALIBRATION | 0.01 SECOND |
| YIG LOCK- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | TRIGGERED | | 0.01 SECOND |
| YIG FM TUNING- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG MAIN TUNING- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG PLL DISABLE- B | GATE | ON/OFF | N/A | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| REFERENCE SIGNAL GENERATOR PS CONTROL/MONITOR | | | | | | | |
| YIG PS DISABLE- A | CONTROL | ON/OFF | N/A | | TRIGGERED | FAULT | 0.01 SECOND |
| YIG PS FAULT- A | FLAG | ON/OFF | N/A | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| YIG PS DISABLE- B | CONTROL | ON/OFF | N/A | | TRIGGERED | FAULT | 0.01 SECOND |
| YIG PS FAULT- B | FLAG | ON/OFF | N/A | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| RSG ALC CONTROL/MONITOR | | | | | | | |
| ALC LEVEL SET- A | CONTROL | ANALOG | 8 BIT | | TRIGGERED | SET-UP | 0.1 SECOND |
| ALC SIGNAL LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC LEVEL SET- B | CONTROL | ANALOG | 8 BIT | | TRIGGERED | SET-UP | 0.1 SECOND |
| ALC SIGNAL LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| RSG FREQ SYNTHESIZER CONTROL/MONITOR | | | | | | | |
| FREQ SYN2 LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FREQ SYN2 LOCK- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FREQ SYN2 TUNE- A | CONTROL | PAR W/STROBE | 8 BIT | ADDRESSABLE BYTES | TRIGGERED | SET-UP | 0.1 SECOND |
| FREQ SYN2 LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FREQ SYN2 LOCK- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FREQ SYN2 TUNE- B | CONTROL | PAR W/STROBE | 8 BIT | ADDRESSABLE BYTES | TRIGGERED | SET-UP | 0.1 SECOND |
| GUNN OSCILLATOR CONTROL/MONITOR | | | | | | | |

## ANTENNA REFERENCE SIGNAL SOFTWARE FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| GUNN DISABLE- A | GATE | ON/OFF | N/A | | TRIGGERED | FAULT | 0.01 SECOND |
| GUNN OSC SELECT- A | CONTROL | UNDEFINED | 8 BIT | | | | |
| GUNN VOLTAGE- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| GUNN CURRENT- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| GUNN FAULT- A | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| GUNN DISABLE- B | GATE | ON/OFF | N/A | | TRIGGERED | FAULT | 0.01 SECOND |
| GUNN OSC SELECT- B | CONTROL | UNDEFINED | 8 BIT | | | | |
| GUNN VOLTAGE- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| GUNN CURRENT- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| GUNN FAULT- B | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| GUNN OSCILLATOR PHASELOCK SERVO | | | | | | | |
| GUNN FINE TUNE- A | CONTROL | ANALOG | 16 BIT | TIME SENSTIVE | CONTINUOUS | | 0.01 SECOND |
| GUNN MAIN TUNE- A | CONTROL | P-MAC | | MOTOR CONTROL | | | |
| GUNN BACKSHORT- A | CONTROL | P-MAC | | MOTOR CONTROL | | | |
| GUNN IF GAIN (LO)- A | CONTROL | ANALOG | 8-BIT EQUIV | TABLE DRIVEN | | | |
| GUNN IF GAIN (HI)- A | CONTROL | ANALOG | 8-BIT EQUIV | TABLE DRIVEN | | | |
| GUNN PLL ERROR- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | | | |
| GUNN PLL DISABLE- A | GATE | ON/OFF | N/A | | TRIGGERED | | 0.01 SECOND |
| GUNN LOCK- A | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| GUNN FINE TUNE- B | CONTROL | ANALOG | 16 BIT | TIME SENSTIVE | CONTINUOUS | | 0.01 SECOND |
| GUNN MAIN TUNE- B | CONTROL | UNDEFINED | UNDEFINED | MOTOR CONTROL | | | |
| GUNN BACKSHORT- B | CONTROL | P-MAC | | MOTOR CONTROL | | | |
| GUNN IF GAIN (LO)- B | CONTROL | ANALOG | 8-BIT EQUIV | TABLE DRIVEN | | | |
| GUNN IF GAIN (HI)- B | CONTROL | ANALOG | 8-BIT EQUIV | TABLE DRIVEN | | | |
| GUNN PLL ERROR- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | | | |
| GUNN PLL DISABLE- B | GATE | ON/OFF | N/A | | TRIGGERED | | 0.01 SECOND |
| GUNN LOCK- B | MONITOR | ANALOG | 8-BIT EQUIV | TIME SENSITIVE | CONTINUOUS | | 10/SECOND |
| GUNN DDS CONTROL/MONITOR | | | | | | | |
| GUNN DDS FREQ- A | CONTROL | VXI BUS | 8 BIT | ADDRESSABLE BYTES | TRIGGERED | SET-UP | 0.01 SECOND |
| GUNN DDS PHASE- A | CONTROL | VXI BUS | 12 BIT | TIME CRITICAL | STROBED | | 0.01 SECOND |
| GUNN DDS FM- A | CONTROL | VXI BUS | 16 BIT | TIME CRITICAL | STROBED | | 0.01 SECOND |
| GUNN DDS LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| GUNN DDS FREQ- B | CONTROL | VXI BUS | 8 BIT | ADDRESSABLE BYTES | TRIGGERED | SET-UP | 0.01 SECOND |
| GUNN DDS PHASE- B | CONTROL | VXI BUS | 12 BIT | TIME CRITICAL | STROBED | | 0.01 SECOND |
| GUNN DDS FM- B | CONTROL | VXI BUS | 16 BIT | TIME CRITICAL | STROBED | | 0.01 SECOND |
| GUNN DDS LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| HARMONIC MIXER CONTROL/MONITOR | | | | | | | |
| HARM MIXER IF SW | CONTROL | UNDEFINED | UNDEFINED | | | | |
| HARM MIXER REF SW | CONTROL | UNDEFINED | UNDEFINED | RELAY DRIVER | | | |
| HARM MIXER BIAS SW | CONTROL | UNDEFINED | UNDEFINED | | | | |

ANTENNA REFERENCE SIGNAL SOFTWARE FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| MAIN POWER SUPPLY CONTROL/MONITOR | | | | | | | |
| MAIN PS +18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |

ANTENNA SHELTER IF SIGNAL SOFTWARE FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| LASER TRANSMITTER CONTROL/MONITOR | | | | | | | |
| FO XMTR TEMP- A | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO XMTR HTR PWR- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR OPT MON- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR LASER- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR THERMAL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR MOD- A | GATE | ON/OFF | N/A | TIME SENSITIVE SAFETY | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR OVRTMP- A | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR DISABLE- A | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR SHUTTER- A | GATE | ON/OFF | N/A | TIME SENSITIVE SAFETY | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR TEMP- B | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO XMTR HTR PWR- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR OPT MON- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR LASER- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR THERMAL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO XMTR MOD- B | GATE | ON/OFF | N/A | TIME SENSITIVE SAFETY | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR OVRTMP- B | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR DISABLE- B | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| FO XMTR SHUTTER- B | GATE | ON/OFF | N/A | TIME SENSITIVE SAFETY | TRIGGERED | FAULT | 0.01 SECOND |
| TOTAL PWR DETECTOR CONTROL/MONITOR | | | | | | | |
| TPD CONTR LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| TPD MEAS LEVEL- A | MONITOR | ANALOG | 16-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| TPD TEMP- A | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| TPD HTR PWR- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| TPD CONTR LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| TPD MEAS LEVEL- B | MONITOR | ANALOG | 16-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| TPD TEMP- B | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| TPD HTR PWR- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| RECEIVER ALC CONTROL/MONITOR | | | | | | | |
| ALC LEVEL SET- A | CONTROL | PAR W/STROBE | 8 BIT | | TRIGGERED | | 0.1 SECOND |
| ALC SIGNAL LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC LEVEL SET- B | CONTROL | PAR W/STROBE | 8 BIT | | TRIGGERED | | 0.1 SECOND |
| ALC SIGNAL LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| DIGITAL ATTENUATOR CONTROL/MONITOR | | | | | | | |
| DIGITAL ATTEN SET- A | CONTROL | PAR W/STROBE | 8-BIT | | TRIGGERED | | 0.1 SECOND |
| DIGITAL ATTEN SET- B | CONTROL | PAR W/STROBE | 8-BIT | | TRIGGERED | | 0.1 SECOND |
| MAIN POWER SUPPLY CONTROL/MONITOR | | | | | | | |
| MAIN PS +18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |

## ANTENNA SHELTER IF SIGNAL SOFTWARE FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| MAIN PS +18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |

CONTROL BUILDING IF SIGNAL SOFTWARE FUNCTIONS

| TITLE | FUNCTION | TYPE | PRECISION | NOTES | OCCURENCE | MODE | TIMING |
|---|---|---|---|---|---|---|---|
| FIBEROPTIC RCVR CONTROL/MONITOR | | | | | | | |
| FO REC LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO RCVR TEMP- A | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO RCVR HTR PWR- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO REC LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| FO RCVR TEMP- B | MONITOR | THERMISTOR | 8-BIT EQUIV | RESISTANCE MEAS | CONTINUOUS | | 1/SECOND |
| FO RCVR HTR PWR- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| IF ALC CONTROL/MONITOR | | | | | | | |
| ALC LEVEL SET- A | CONTROL | ANALOG | 8 BIT | | TRIGGERED | SET-UP | 0.1 SECOND |
| ALC SIGNAL LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- A | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC LEVEL SET- B | CONTROL | ANALOG | 8 BIT | | TRIGGERED | SET-UP | 0.1 SECOND |
| ALC SIGNAL LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| ALC ATTEN LEVEL- B | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| DIGITAL ATTENUATOR CONTROL/MONITOR | | | | | | | |
| DIGITAL ATTEN SET- A | CONTROL | ANALOG | 8-BIT | | | | |
| DIGITAL ATTEN SET- B | CONTROL | ANALOG | 8-BIT | | | | |
| MAIN POWER SUPPLY CONTROL/MONITOR | | | | | | | |
| MAIN PS +18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS -18 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 V | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 I | MONITOR | ANALOG | 8-BIT EQUIV | | CONTINUOUS | | 1/SECOND |
| MAIN PS +8 FAULT | FLAG | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS -18 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |
| MAIN PS +8 DISABLE | GATE | ON/OFF | N/A | TIME SENSITIVE | TRIGGERED | FAULT | 0.01 SECOND |