Submillimeter Array Technical Memorandum

Number. 82
Date 12/13/1994
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Improving the Frequency Resolution of the SMA Correlator

I. Introduction

It has been suggested that the frequency resolution capability of the SMA correlator will limit some observations. Therefore, we have considered some methods to increase the frequency resolution. This paper will examine the engineering aspects of these modifications, given the present advanced state of the correlator design. The proposed methods avoid major modifications to the architecture and instead consider possibilities that would minimally impact the present design.

To avoid major rework, these solutions do not directly change the number of lags in the correlator. Instead, they will extend the usual trade-off between processed bandwidth and frequency resolution. Therefore, all these approaches will decrease the total processed bandwidth by a factor related to the increase in frequency resolution.

The frequency resolution of an XF correlator is limited by the depth of it's lag chain. The following equation describes the frequency resolution of the SMA correlator in interferometer mode: In

$$Freq.\ Res = \frac{(Samp.\ Freq. \times Demux\ Factor \times Window\ Factor)}{Total\ No.\ Lags}$$

In the case of the SMA, the normal lag chain is constrained to a single correlator board, which holds 32 correlator chips. Consequently, the maximum number of lags available to process a *chunk'* is 16K (5 12 lags per chip). However, to utilize all 16K lags would require dumping a baseline, which is doubtlessly unacceptable for most experiments. Therefore, the maximum number of lags which can be used is reduced to 8K. Unfortunately, in many observations, this would be reduced by another factor of 2 to get both receiver channels, which coexist on the same correlator board. (This arrangement is necessary to implement cross-polarization measurements). Consequently, inserting the pertinent numbers gives a best-case frequency resolution of 203 kHz for a single receiver or 406 kHz for dual receiver observing. These numbers were calculated using the SMA sampling frequency of 208 MHz, demux factor of 4, a *window factor* of 2 (Hanning window)[1], and are for interferometric operation. In single dish observations, the frequency resolution will be inherently better by a factor of 4, without any loss in bandwidth.

It is worth noting that a simple and direct improvement in frequency resolution can be made by adjusting the data windowing (or weighting). By using a Bartlett window, the window factor can be reduced to 1.77. Or better still, a rectangular window reduces the window factor to 1.2. This improvement in frequency resolution comes at the expense of bigger sidelobes. However, in some

1. A "chunk" refers to a section of the correlators processed spectrum, which is derived from a single sampler. Normally, a chunk is 82 MHz wide.

observations, this might be an acceptable trade-off.

The rest of the discussion will consider some techniques for increasing the frequency resolution by increasing the effective number of lags applied to a chunk. Also provided are rough estimates of the cost (both direct and indirect) for these proposals. However, several of these proposals require changes to hardware which must be initiated quite soon. If these changes are not made very soon, the total cost will increase to include any necessary rework.

II. **Resolution Improvement Options**

II. 1. **Analog Filtering**

This approach attacks the problem by decreasing the demux factor. The demux factor is easily reduced from 4 to 2 using the existing data switches. As a consequence, every other data sample from a chunk's sampled data stream is tossed in the bit bucket. This reduces the effective sample rate by 2. Unfortunately, this also violates the Nyquist theorem and causes aliasing (folding) of the spectrum. To avoid aliasing, we must introduce an extra filter to attenuate the image spectrum (and its noise).

Thus, the analog signal processing must include some additional filters and RF switches. It would not be necessary to provide this filter for every chunk in the SMA correlator (288 total). Although there would be some loss in homogeneity, it would be possible to operate with only 72 additional filters and switches. This would cost roughly $15K in parts and extra packaging. In terms of manpower, this solution would require about one month of engineering time (selecting, purchasing and testing the filter), plus two months of additional technician effort during construction. To implement the additional modes will require a few weeks of programming time, but this will be needed in all cases, so should not affect the comparison.

This scheme will increase the best frequency resolution by 4 (Samp. Freq. = 104 MHz, Demux Factor = 2). This bandwidth of this chunk is reduced by more than 2, due to filter rolloff. A reasonable estimate of the usable chunk bandwidth in the high resolution mode is 30 MHz, versus the usual 82 MHz. The problem of filter roll-off would also severely limit any additional improvements to the frequency resolution. Thus, although it would be possible to improve the resolution by a factor of 16 (by dropping the demux factor to 1), the usable bandwidth would decrease to a very modest number like 5 MHz. Naturally, this would also require an additional filter, which would require a rather steep rolloff.

The use of an analog filter is a very direct and simple approach with little inherent risk. However, it does increase the number of analog components in the signal path and has a slight chance of affecting stability and reliability. In particular, the relative steepness (in amplitude) of the filter and it's phase structure (which will be worse than the standard 82 MHz filter) could be an issue.

11.2. **Digital Filter**

This scheme is very similar to the analog filter method just described. The improvement in frequency resolution is achieved by lowering the demux factor and the effective sample rate. The difference is in the implementation of the anti-alias filter. Instead of an analog filter, it might be possible to use a digital filter placed on the delay board. The design of the filter coefficients is quite simple and it could be implemented in an FPGA, much like the delay unit. In fact, the digital filter will be more gradual than the analog filter because of offset sampling.

However, there is some additional complexity due to the severe quantization of the data. This issue will necessitate some software simulations to examine the effects of quantization.

If the filter is implemented in the FPGA chips, the only direct cost would be the use of a larger (and costlier) FPGA chip. A rough guess as to the incremental cost is $40 per device, which gives a system cost of $4K (assuming this is done to only 72 data paths). However, this approach requires a moderate amount of engineering time to ensure there are no unforeseen consequences of the quantization, a rough guess of the engineering time required is 3 months. There are also commercially available chips which can be considered, but an examination of their quantization scheme will still be needed.

This approach has several advantages, include the possibility of no physical changes to the present system. The FPGA's are generally interchangeable, so a higher density device could be substituted without altering the layout. Also, most of the design work could be postponed to a later date with this scheme and thereby avoid delays in producing the prototype. The digital filter should be predictable, and therefore not introduce any stability or calibration problems. The primary negative of this approach is the moderate amount of extra engineering time.

II.3. Lag Split

This method would not alter the demux rate, but increase the number of lags by using several correlator boards to process a single baseline. Effectively, this is identical to daisy-chaining correlator boards, except the extra data paths are implemented on the delay boards. This would avoid changes to the correlator architecture and if the extra paths are limited. to the four chunks that reside on a single delay board, there shouldn't be any problems with data synchronization.

In practice, there are two ways that we could subdivide a single correlation calculation. One approach is sketched in Figure #1, where the geometric delay chips are used to insert extra delays. Normally, a given board would calculate all lags: $\{-T < \tau \leq T\}$. By inserting the extra delays, this lag "window" can be shifted to: $\{-2T < \tau < 0\}$. An extra delay in the other antenna's path would shift the delay window to $\{0 < \tau < 2T\}$. Thus the full lag calculation could be separated to two boards and the effective lag window is doubled.

The previous scheme is very simple and direct, but a better method is available for the SMA correlator. To calculate the correlation function of a 4X demultiplexed data signal requires a cross correlation of all pairs of the data samples (or phases) which are available in a given correlator clock. This means a single correlation measurement gets divided into 16 (4x4) separate correlation calculations. Normally all 16 calculations are done on single board, however, using the available crosspoint switching resources, it is possible for one board to perform 1/2 of these calculations with twice the number of lags. Thus, the full correlation can be divided and processed on two boards. This option is sketched in Figure #2.

This scheme has many advantages, it is simple and has little impact on the correlator design. The direct costs are very low (about $1K to implement the extra data paths on the delay board), There is very little risk and the problems of calibration are gone because the same analog filter is used. The primary disadvantage of this method is that it uses more correlator resources. The previous options increased the frequency resolution by tossing bandwidth from the high resolution chunk. This method will consume the resources normally available for other independent chunks.

Another consequence of this option is an increase in programming time. In this mode, the lags from a given chunk are not contained on a single correlator board. Therefore, the programming of the

on-board DSP is somewhat more complicated in order to support this "divided" mode. A rough estimate of programming time is 1 extra month (above and beyond the month already needed to support high resolution modes). Fortunately, this extrawork could be posponsed to a more convenient date.

II.4. **Baseline Split**

This mode is very similar to the previous option (#3) with many of the same properties. In much the same fashion, the correlation calculations that were performed on a single board are divided

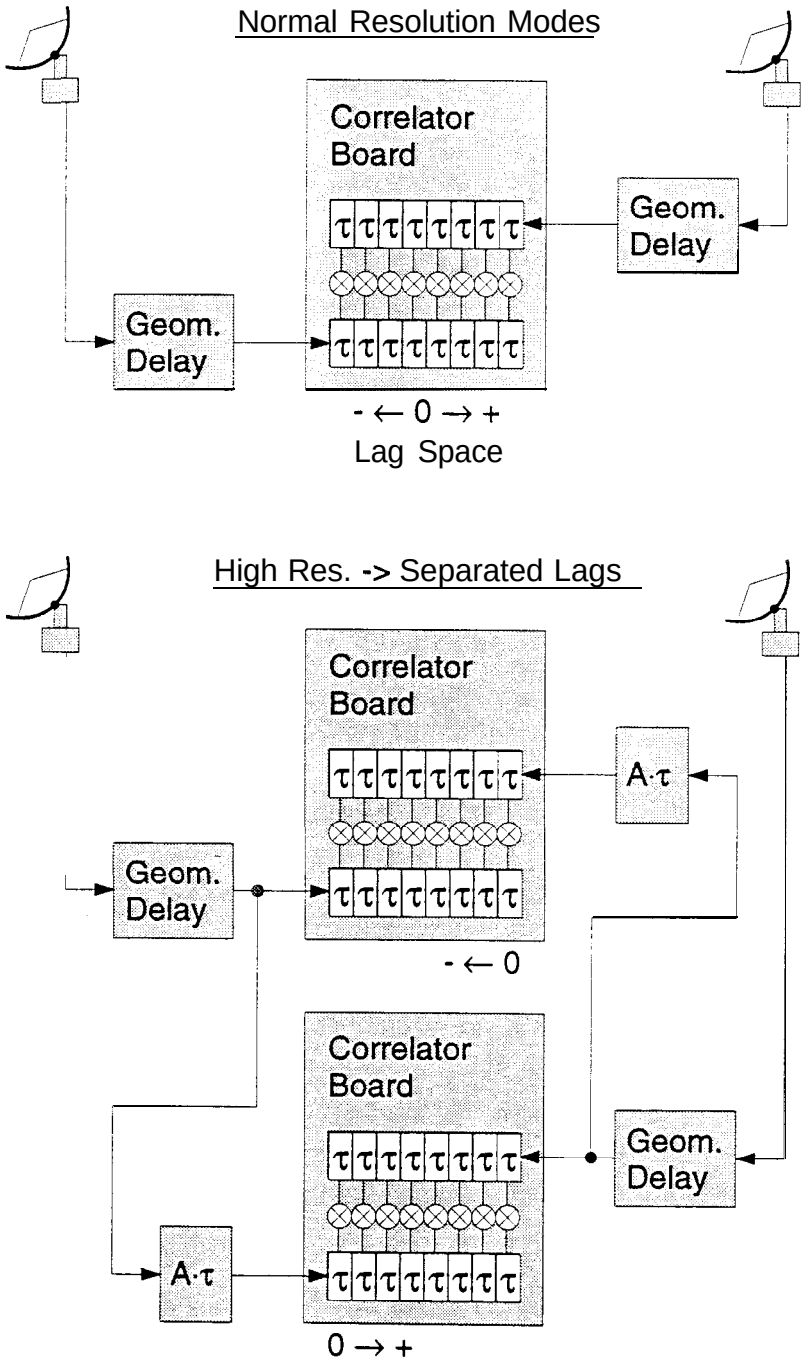

Figure #1 - Lag Split using Lag window shift

and performed on two separate correlator boards. However, unlike the previous option, the board's calculations are segregated by baselines. This aspect will reduce the complexity of programming of the DSP software because a single correlation will remain on a given board. The only practical modifications are the extra wiring on the delay board (just as in option #3).

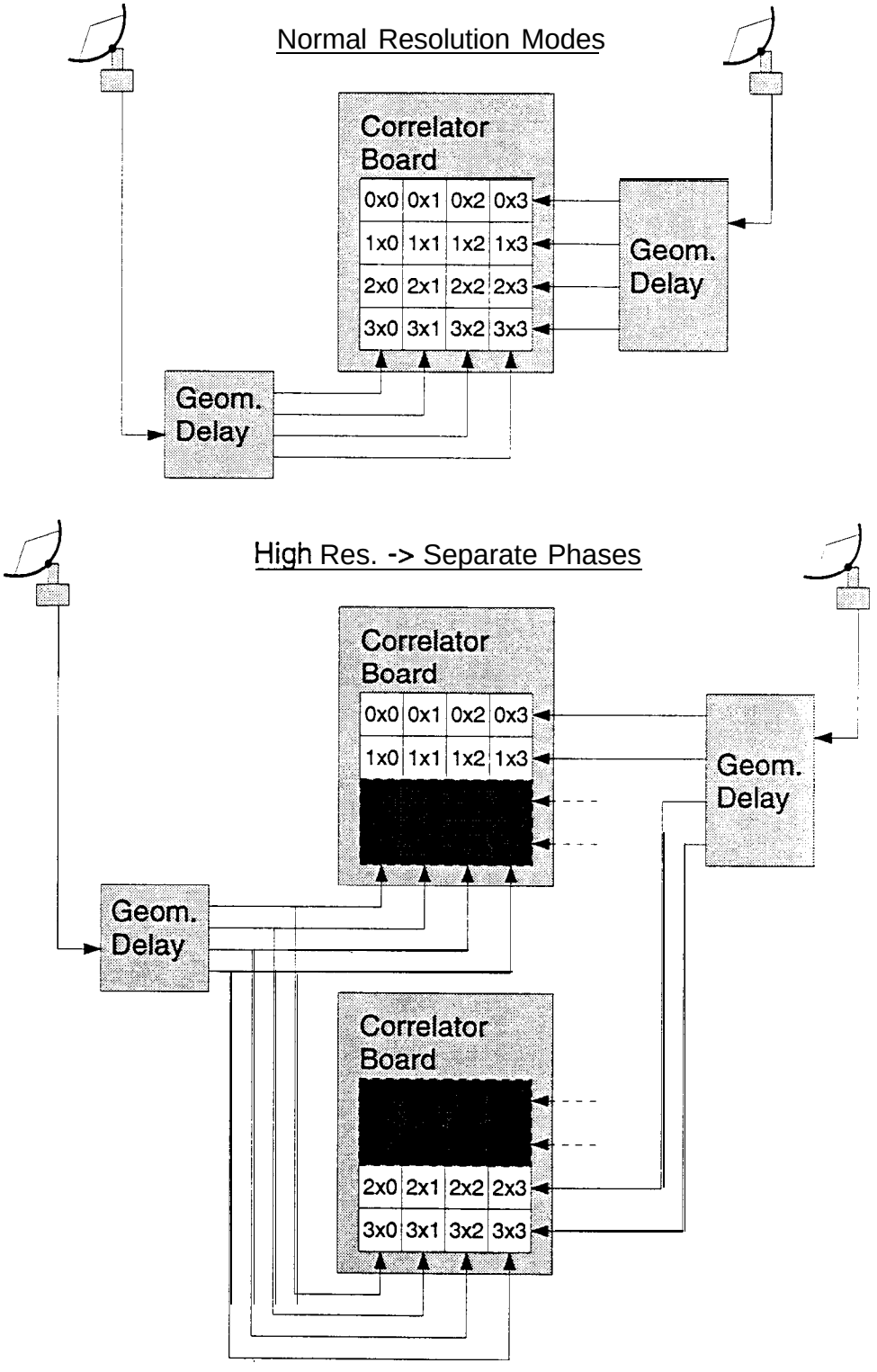

Figure #2 - Lag Split using time samples

Unfortunately, this mode suffers from a severe problem. The ability to redistribute baselines using the present switching arrangement is very limited. At this time, it is not even clear that the necessary switching options are available for a minimum implementation of this option. Even if the necessary switching paths are available (or can be altered before the backplanes are built), this mode will severely limit the flexibility of the correlator in high resolution mode. For example, it is unlikely that the 8 station mode (SMA+JCMT+CSO) will be available at high resolution. The only way to remove this limitation would be to greatly increase the switching resources of the correlator by adding more crosspoint switches between the the delay unit and the correlator boards. At this stage in the development, a major change such as this would seem imprudent.

III. Conclusion

Hardware costs are clearly not the issue. However, given the limitations on manpower for this project, the modest manpower needs can not be ignored. The ultimate decision as to the best approach will require feedback from the potential users of this mode. However, a tentative recommendation would favor option #3 (Lag Split), which can produce the necessary resolution without too much cost or immediate effort. Also, at some later date it would be useful to re-examine Option #2 (Digital Filter) given it's advantage of greater flexibility.

The option discussed are summarized in Table #1.

IV. References

[1] Thompson, Moran, Swenson, "Interferometry and Synthesis in Radio Astronomy", p 239.

Method	Resolution Improvement	#of Hi Res Chunks	Chunk Size	Lags used
1) Analog Filter	x4	6	≈ 30 Mhz	xl
2) Digital Filter	x4	6	= 30 Mhz	x1
3) Split Lags	x2 x4	3 1	82 Mhz	x2 x4
4)Split Baselines	x2	3	82 Mhz	x2

Method	Costs			Positives	Negatives
	Hard-ware ($)	Labor: Now (Months)	Labor: Later (Months)		
1) Analog Filter	15K	3	1	conventional	more calibration, reliability?
2) Digital Filter	4K	3	1	ideal filter	untried
3) Split Lags	1K	-	2	modest effort, little risk	less chunks
4)Split Baselines	1K	1 1/2	1 1/2		not in 8 station

Table 1 - Summary of Options