Signal Transmission and Correlator

- Our engineering limitations
- The present SMA system
- Analog IF and transmission upgrades
- New correlator options
  - What we want
  - Available A/D converters
  - The CASPER approach
  - Custom backplane corner turning
  - Commercial vendors

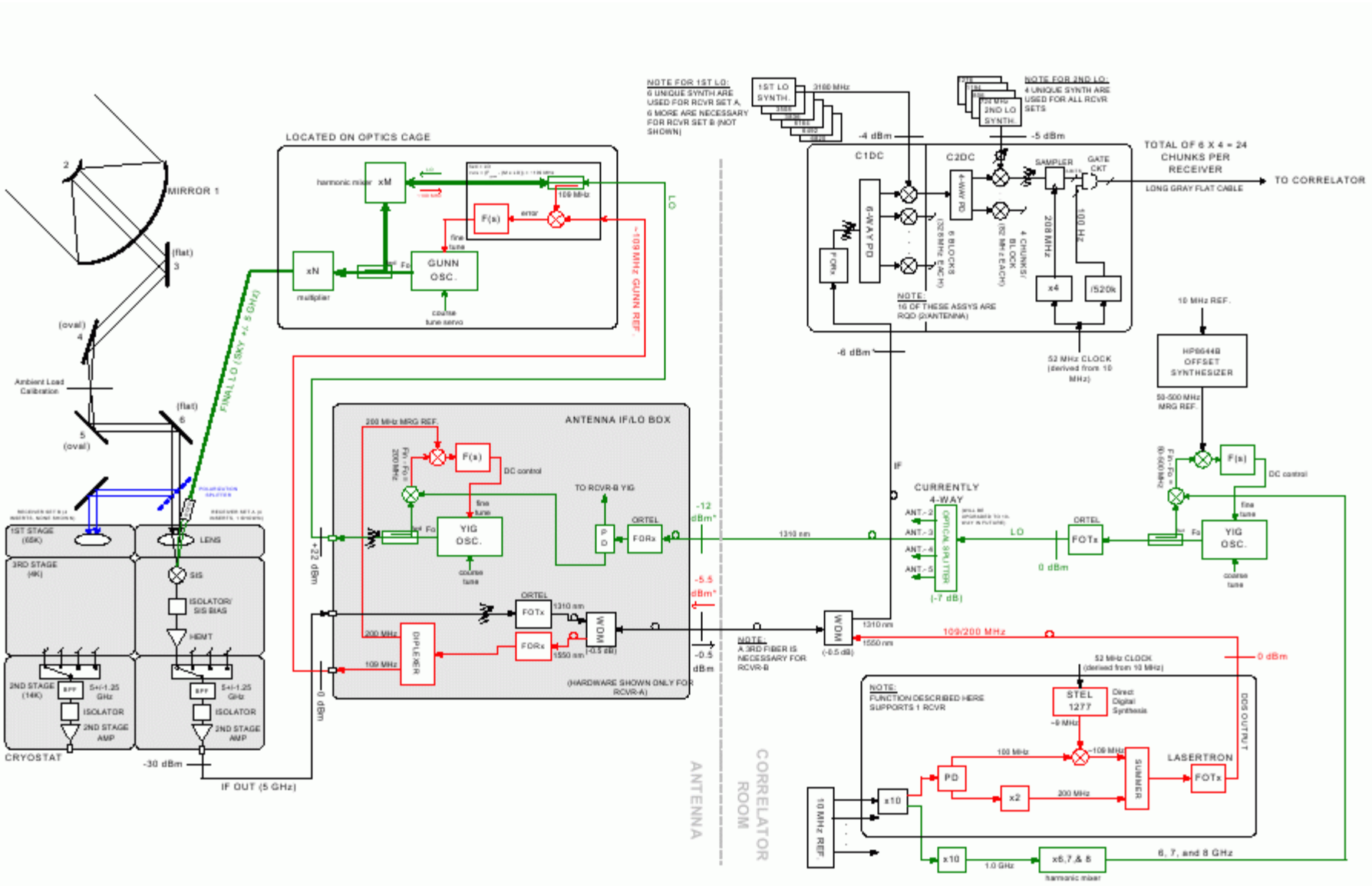

NOTE FOR 1ST LO:
6 UNIQUE SYNTH ARE USED FOR RCVR SET A, 6 MORE ARE NECESSARY FOR RCVR SET B (NOT SHOWN)
1ST LO SYNTH.
3100 MHz
NOTE FOR 2ND LO:
4 UNIQUE SYNTH ARE USED FOR ALL RCVR SETS
2ND LO SYNTH.
-4 dBm
-5 dBm
C1DC
C2DC
SAMPLER
GATE CKT
TOTAL OF 6 X 4 = 24 CHUNKS PER RECEIVER
TO CORRELATOR
LONG GRAY FLAT CABLE
6-WAY PD
4-WAY PD
FORx
6 BLOCKS (32.8 MHz EACH)
4 CHUNKS/ BLOCK (62 MHz EACH)
208 MHz
100 Hz
x4
/5208
NOTE:
16 OF THESE ASSYS ARE REQD (2/ANTENNA)
-6 dBm*
52 MHz CLOCK (derived from 10 MHz)
10 MHz REF.
HP8644B OFFSET SYNTHESIZER
50-500 MHz MRG REF.
LOCATED ON OPTICS CAGE
harmonic mixer xM
109 MHz
F(a)
error
fine tune
xN
multiplier
GUNN OSC.
coarse tune servo
LO
~109 MHz GUNN REF.
FINAL LO (SKY +/- 5 GHz)
MIRROR 1
2
(flat) 3
(oval) 4
Ambient Load Calibration
(flat) 6
5 (oval)
1ST STAGE (65K)
LENS
3RD STAGE (4K)
SIS
ISOLATOR/ SIS BIAS
HEMT
2ND STAGE (14K)
BPF
5+/-1.25 GHz
ISOLATOR
2ND STAGE AMP
CRYOSTAT
-30 dBm
IF OUT (5 GHz)
ANTENNA IF/LO BOX
200 MHz MRG REF.
F(a)
DC control
TO RCVR-B YIG
fine tune
YIG OSC.
coarse tune
PD
ORTEL
FORx
+22 dBm
0 dBm
-12 dBm*
-5.5 dBm*
-0.5 dBm
1310 nm
ORTEL
FOTx
1310 nm
WDM
(~0.5 dB)
200 MHz
DIPLEXER
109 MHz
FORx
1550 nm
(HARDWARE SHOWN ONLY FOR RCVR-A)
NOTE:
A 3RD FIBER IS NECESSARY FOR RCVR-B
WDM
(~0.5 dB)
1310 nm
1550 nm
IF
CURRENTLY 4-WAY
ANT.-2
ANT.-3
ANT.-4
ANT.-5
OPTICAL SPLITTER
(~7 dB)
LO
ORTEL
FOTx
0 dBm
109/200 MHz
0 dBm
52 MHz CLOCK (derived from 10 MHz)
NOTE:
FUNCTION DESCRIBED HERE SUPPORTS 1 RCVR
STEL 1277
Direct Digital Synthesis
~9 MHz
100 MHz
~109 MHz
PD
x10
x2
200 MHz
SUMMER
LASERTRON
FOTx
DDS OUTPUT
10 MHz REF.
x10
1.0 GHz
x6,7,& 8
harmonic mixer
6, 7, and 8 GHz
ANTENNA
CORRELATOR ROOM

Table 1. User requirements for SMA wideband correlator.

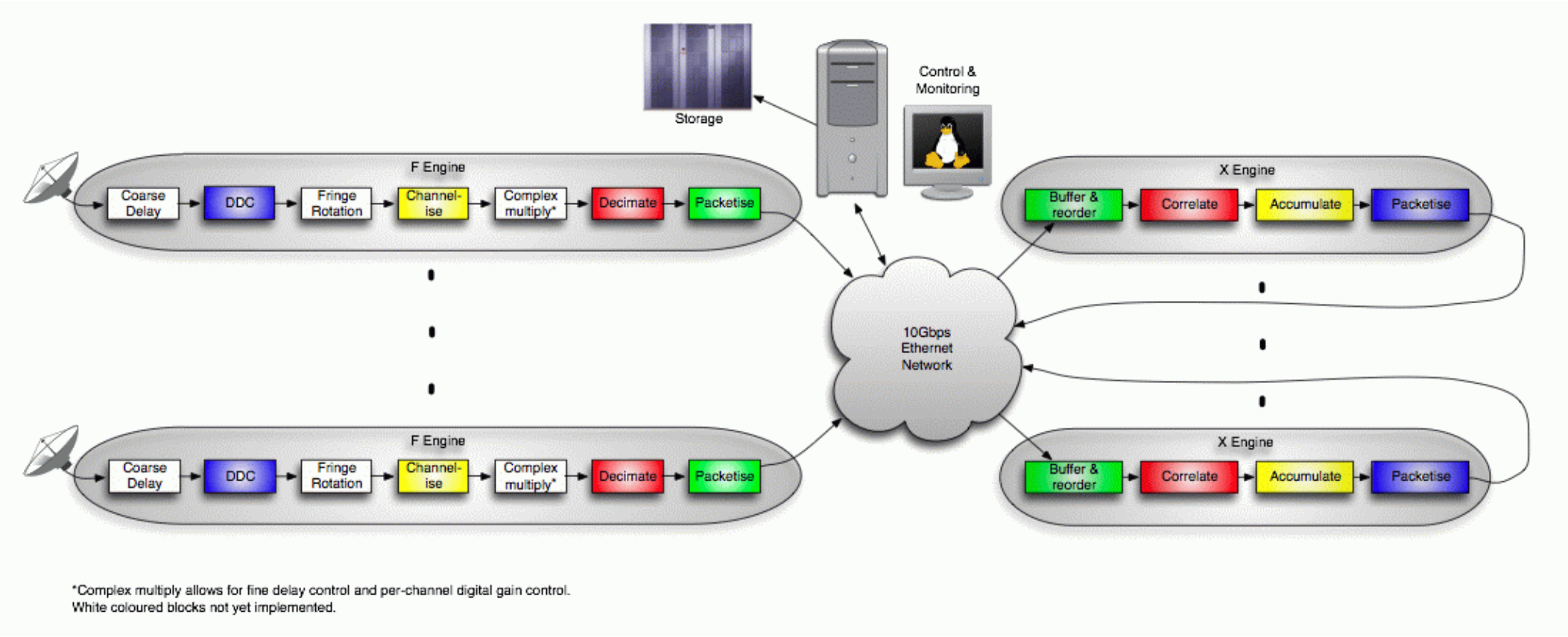
feature	full offering	initial release	remarks
number of antennas	8		2 Rx each. eSMA support?
total bandwidth	18 GHz	9 GHz	for each of two receivers
number of sidebands	2		upper and lower 18 GHz each
simultaneous receivers	2	1	dual freq. or dual pol. 230 & 345 GHZ
# baselines	56	28	28 per Rx, full Stokes
finest continuum resolution	0.5 MHz		16,384 channels / 9 GHz block
coarsest continuum resolution	70.3 MHz		128 channels / 9 GHz block
finest spectral line res.	25 kHz		best possible SMA res
# spectral bands	12		maximum simultaneous hires bands
zooming band width	500 MHz		widest single spectral line
fastest dump rate	0.65 s		single full Walsh cycle
dynamic range	30 dB		weak spectral line near strong
baseline to baseline isolation	30 dB		crosstalk from baseline to baseline
sideband isolation	25 dB		crosstalk USB <—>LSB
maximum baseline delay	2 km		assumes current SMA configuration
# simultaneous autocorrelations	16		Can autocorrelate each antenna
phased array bandwidth	8 GHz	4 GHz	4 GHz × dual pol.
celestial holography mode			might need faster dump

f_s (GSa/s)	BW (GHz)	# bits	Manuf.	Part #	~cost	remarks
5	2.0	8	e2v	EV8AQ160	$300	ASIAA board H. Jiang
12.5	8	8	Maxtek	—	$17k	mature module
20	8	5	e2v	EV5AS210	$7k	Torres et al., IRAM, 8Gsps
20	13	8	Agilent	—	—	
26	26	3+ oflow	Hittite	—	$8k	'rumored' @ ~$8k
30	14	6	Micram	ADC30	$10k	only demo 12 GSa/s
56	15	8	Fujitsu	CHAIS	—	snapshot, no stream
20	10	1	Hittite	HMC874LC3C	$40	clocked comp, no demux
12.5	14	1	Inphi	1385DX	—	latched comp, 1:8 demux
25	18	1	Inphi	25707CP	—	latched comp, no demux

ADC Sample Rate	Chunk Width	# Chunks per antpol	Total Chunks
5	2	9	144
10	4.5	4	64
14	6	3	48
20	9	2	32

Our current IF processor has 384 chunks

CASPER



- One 10GbE will carry ~ 8 Gb/s, at 4 bits/sample -> 2Gs/s or 1 GHz
- There could be 19 separate 10GbE switches
- Each switch would have 16 inputs (using a standard trick of feeding the F engines through the X engines to exploit the bidirectionality of the ports).
- Total 608 ports @ $200/port -> $1.2M

Specialized Backplane for Corner Turning

- This is the approach CARMA and PdBI are using.
- A Vertex 6 has a large number of LVDS ports which can be routed in a backplane.
- Each backplane would need to support 16 station cards and some number of X engines.
- There would be 2-9 back planes depending on the ADC sampling rate.
- In the case of 9 analog channels there might be only 9 station cards.

Summary

- We have limited ability to design high speed digital cards or produce large numbers of Analog channels.
- The situation with high speed A/D converters is unclear now, but several are promised.
- The CASPER approach is appealing. It is being used by other large projects (MeerKat and PAPER).
- For large systems a more custom system design such as Dave Hawkins is doing may be advantageous. We are looking into what he is doing. His designs are motivated by reusing existing hardware, though.
- There are companies who design systems with state of the art FPGAs. We are talking to one.
- See more on the poster by Jonathan Weintroub and Rurik Primiani in the control room or ask for a lab demo.