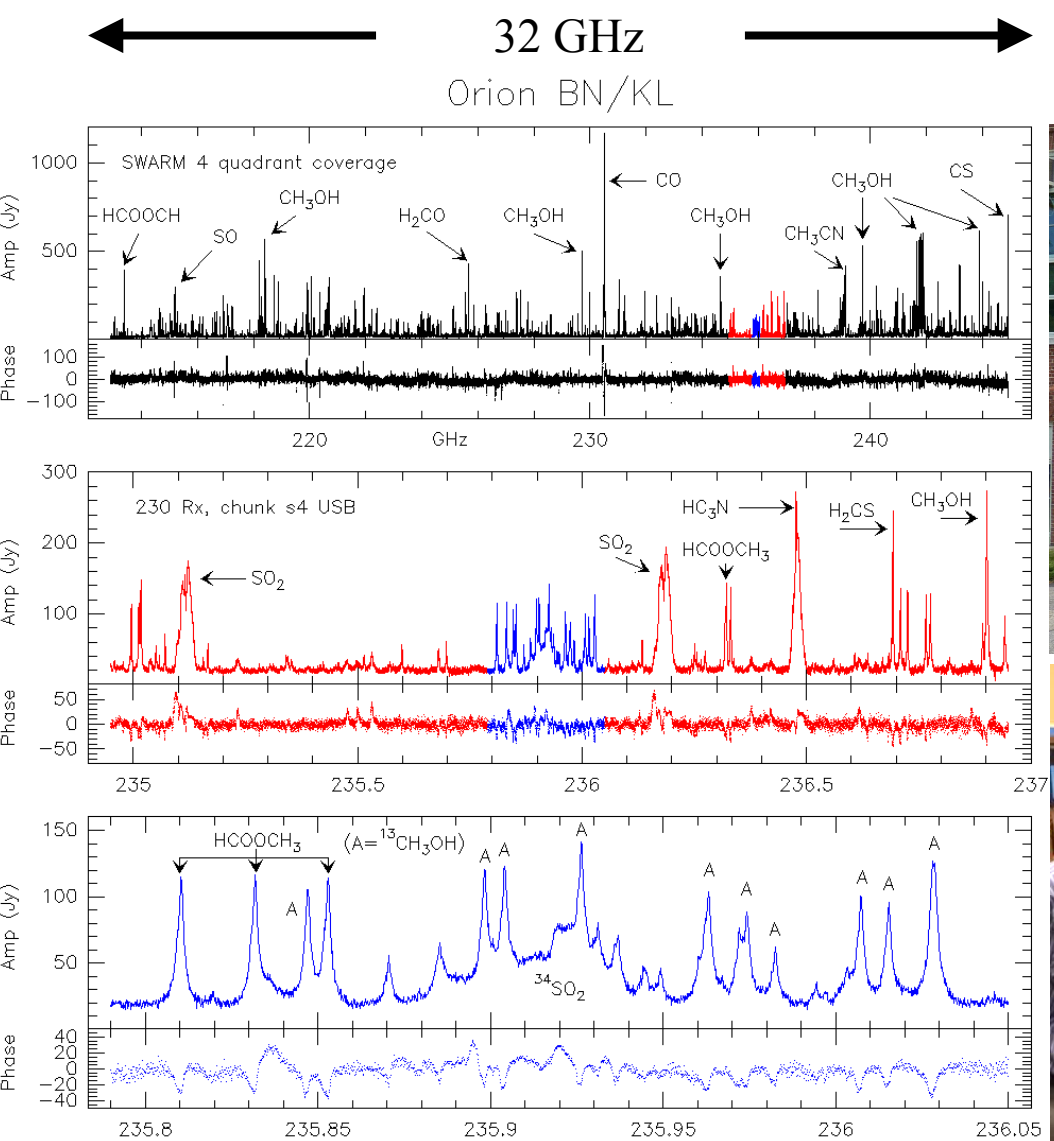
SWARM 2.0: Future Wideband Digital Technology for wSMA



Jonathan Weintroub

SAO/CfA

SMA Visiting Committee

18 July 2018

Technology evolution: SWARM (actual) to wSMA (planned)

	SWARM (32 GHz)	*wSMA (128 GHz)*
sampled bandwidth	2 GHz *(64 IF blocks, 8/antenna)*	8 GHz *(64 IF blocks, 8/antenna)*
FPGA family	Virtex 6 SX475T *(2016 multipliers, 0.5M logic cells)*	Ultrascale+ VU9P *(6,840 multipliers, 2.8M logic cells)*
Ethernet data rate	10 Gbps	100 Gbps
Sampler/ADC location	Control building	Antennas

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Tracking ADCs with sample rates > 5 Gsps

Table 1: Summary table of high speed ADC parts, WiP, contributions welcome, JW, July 16, 2018

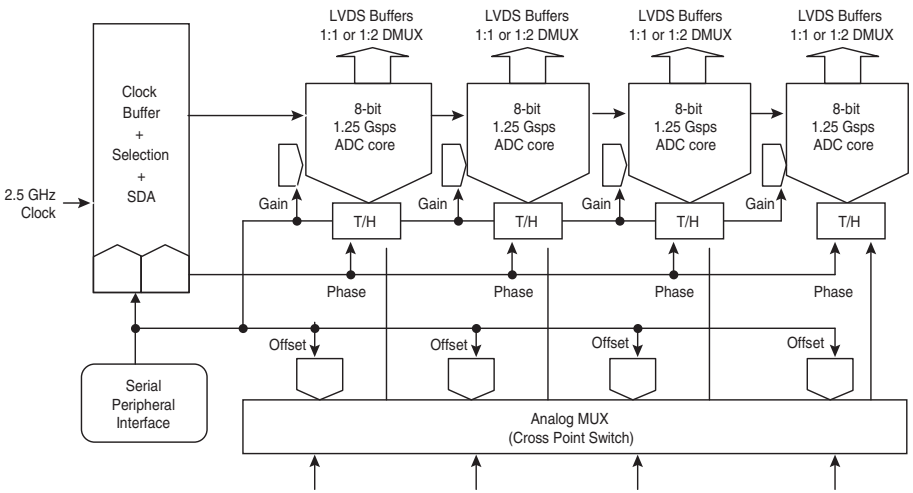
f_s (GSa/s)	cores	BW (GHz)	bits	Manuf.	Part #	~cost	remarks
5	4	2.0	8	e2v	EV8AQ160	$300	ASIAA/Jiang SWARM
6.4	4	>10	12	TI	ADC12DJ3200	$2196	COTS in stock
10.25	>4	6.5	12	Analog Dev	AD9213	$6451	COTS
12	1	20	4	Adsantec	ASNT7120-KMA	$800	3.5 ENOB, 2W, ZDOK
12.5		8	8	Tektronix Comp.	—	$17k	formerly Maxtek
15	1	20	4	Adsantec	ASNT7122-KMA	$1.9k	7120 w/ SERDES, PRBS
16	1	20	4	Adsantec	ASNT7123-KMA	$?	clock optimized 7122
20	4/2	8	5	e2v	EV5AS210	$7k	used for NOEMA, discont.
20		13	8	Keysight	—	—	
20	1	10	3+oflow	Analog Dev.	HMC5401LC5	$2,863	was Hittite, SAO eval. bd.
20	4/5		6	Pacific Microchip	SBIR	$3-5k	JESD204B, Esistream
25	1	22	4	Alphacore	A4B25G		w/ SERDES,
25	1	22	4	Alphacore	A6B25G		w/ SERDES,
34	4	20+	6	Micram	ADC3401/2	$47k	module, ADC30 old price
56	64	20	8	Pacific Microchip	SBIR	$3-5k	avl Q1 2019
56		13	68	Guzik	WDM5121	—	snapshot, 4 Gpt memory
42 - 68		25	10	Jariet	Williamson ADC	$??	ASIC IP macro only, NDA
56	320	15	8	Fujitsu	Robin/Blackbird	$20k	CHAIS, Vadatech
20	1	10	1	Hittite	HMC874LC3C	$40	clocked comp, no demux
12.5	1	14	1	Inphi	1385DX	—	latched comp, 1:8 demux
25	1	18	1	Inphi	25707CP	—	latched comp, no demux

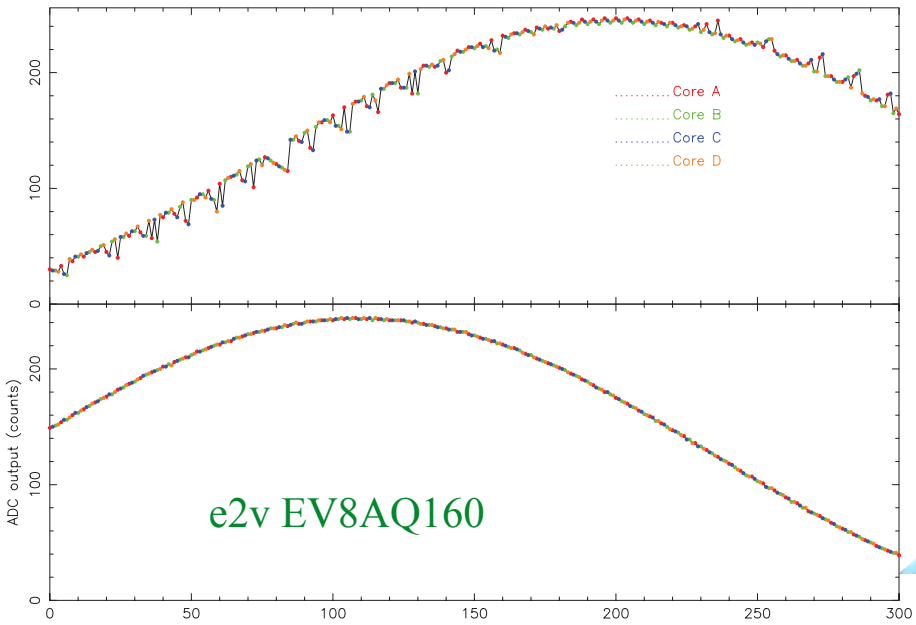
- Market is quite sparse
- Single core is very attractive
- >4 cores is scary
- Some of the pricing is crazy

SWARM: 5 GSa/s sampler, ROACH2 and 10 Gb/s Ethernet

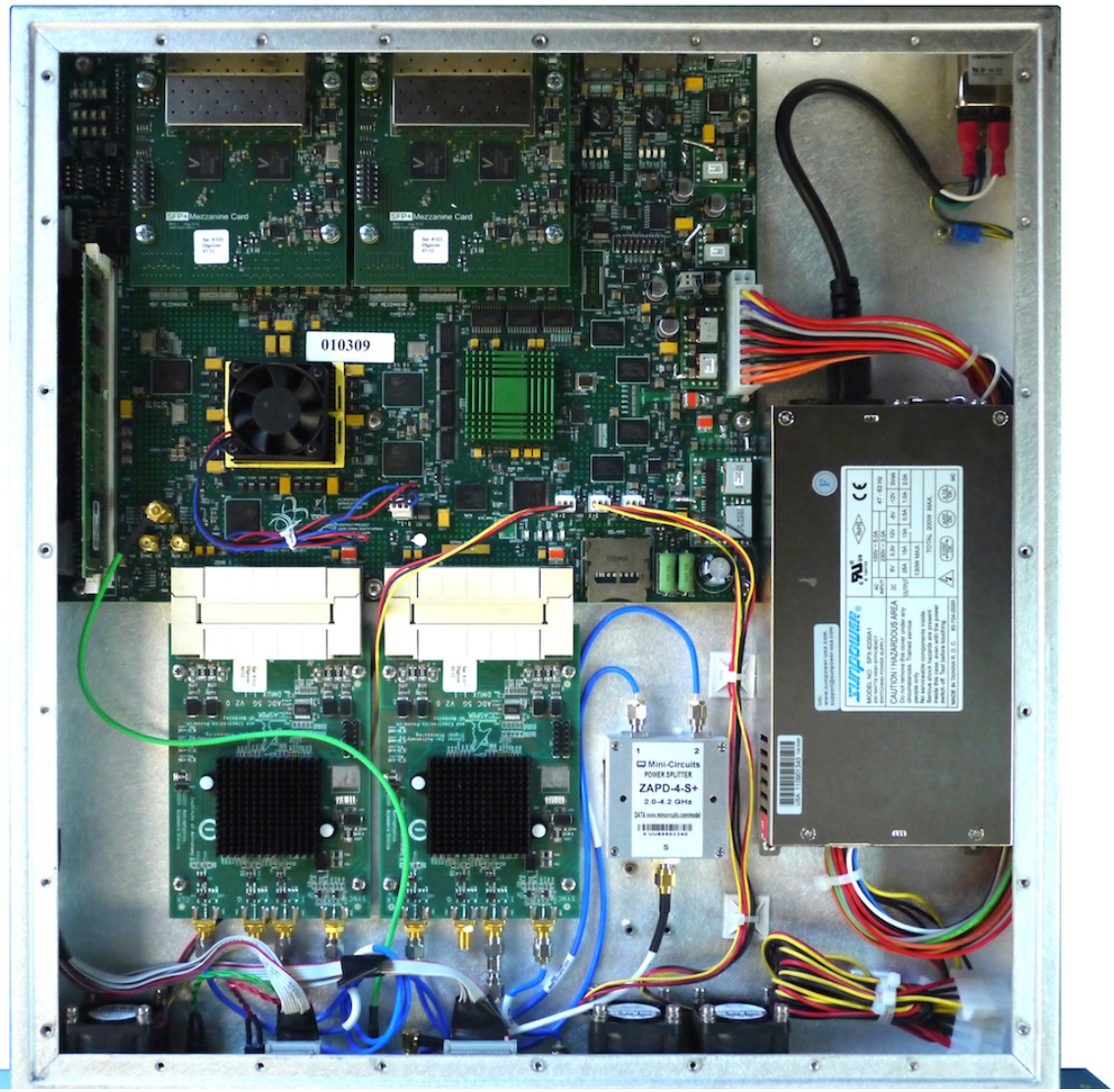
(Jiang et al., PASP 126, 761; 2014; Patel et al., JAI 3, 1 2014, Primiani et al)

Ultra Fast Analog-to-Digital Converters are typically interleaved multi-core devices
This introduces interleaving artifacts which must be calibrated





CASPER ROACH2 with Dual ASIAA ADCs
as configured for SWARM
Photo by Derek Kubo

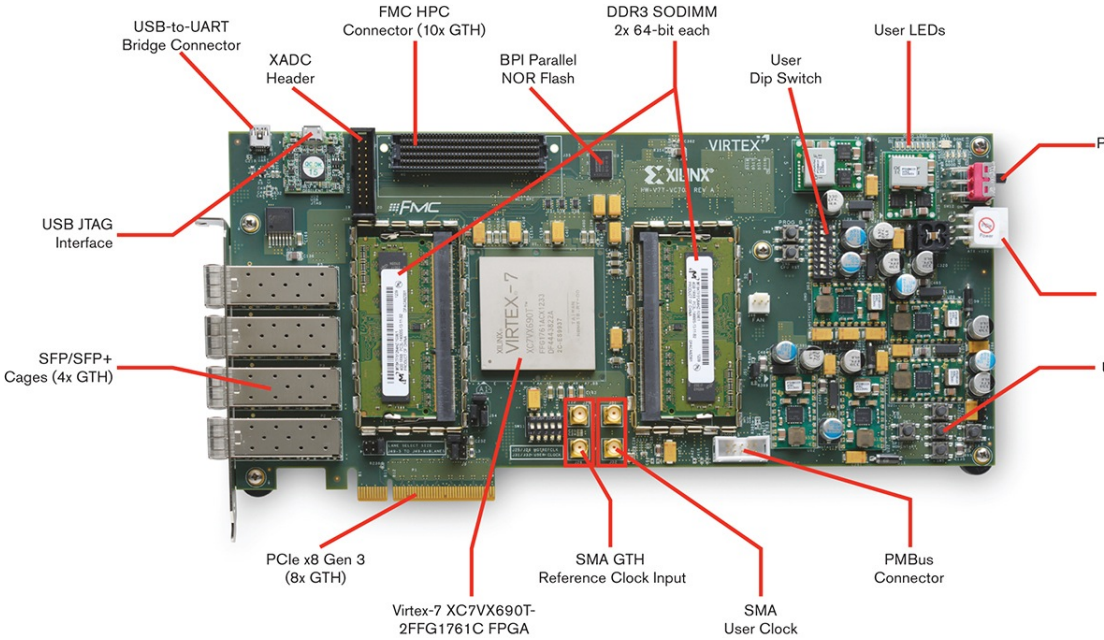


(For more on CASPER see Hickish et al., JAI, 2016)

SAO 20 GS/s ADC based on Hittite HMCAD5831LP9BE, single core

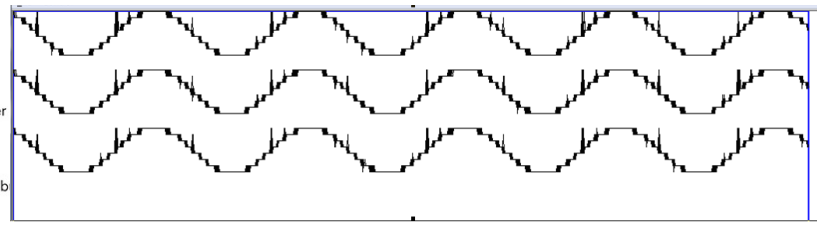
(Weintroub and Raffanti, ISSTT, 2015)

Funded by SI Competitive Grants Program for Science

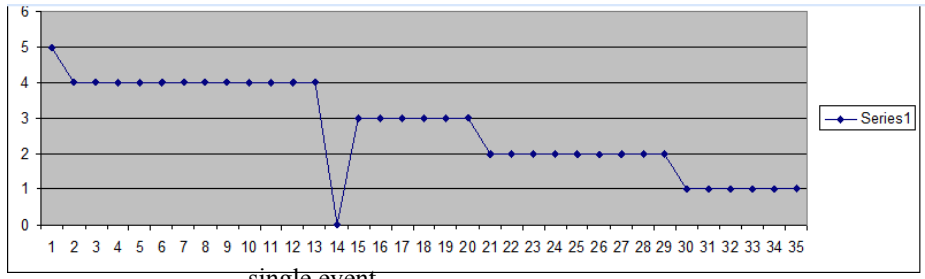


VC709 Xilinx V7 Evaluation Board
bargain basement price: $4995

"sparkle codes" ~ 1 in 1000 frequency



persistence display



single event

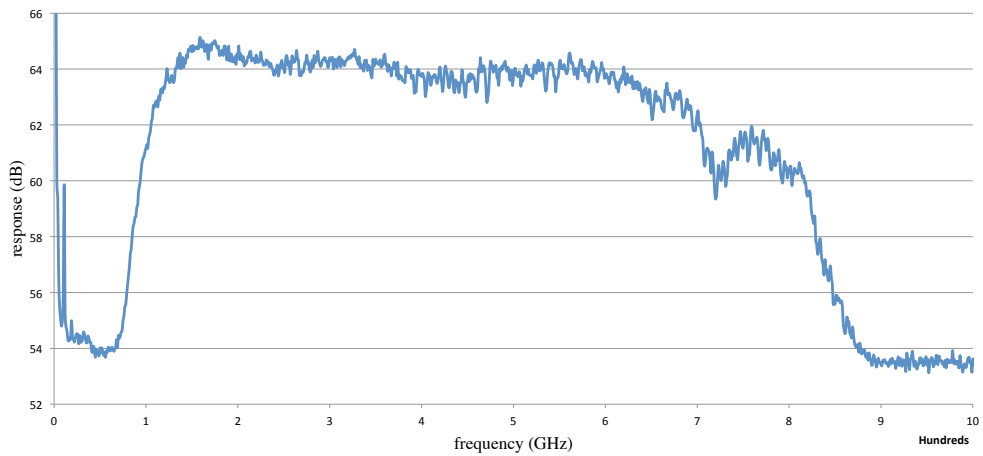
SERDES Transceivers:
GTP, GTX, GTH, GTZ

GTH features:

- 7 tap decision feedback equalizer (DFE) vs 5-tap for GTX
- Rx reflection cancellation
- In the Tx, the "Phase Interpolator PPM Controller" which allows fine-grain adjustment of the Tx phase

2 to 8.2 GHz Noise passband

power spectrum of 3-bit sampled noise

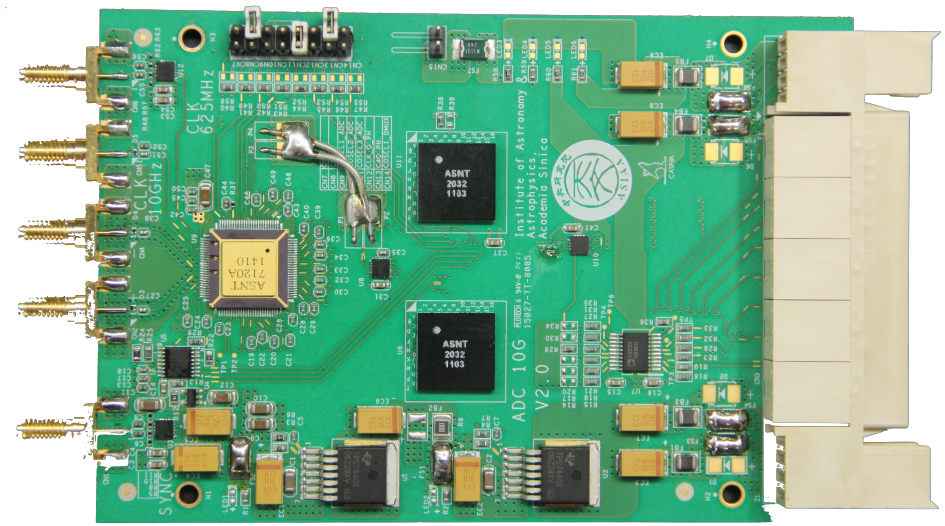


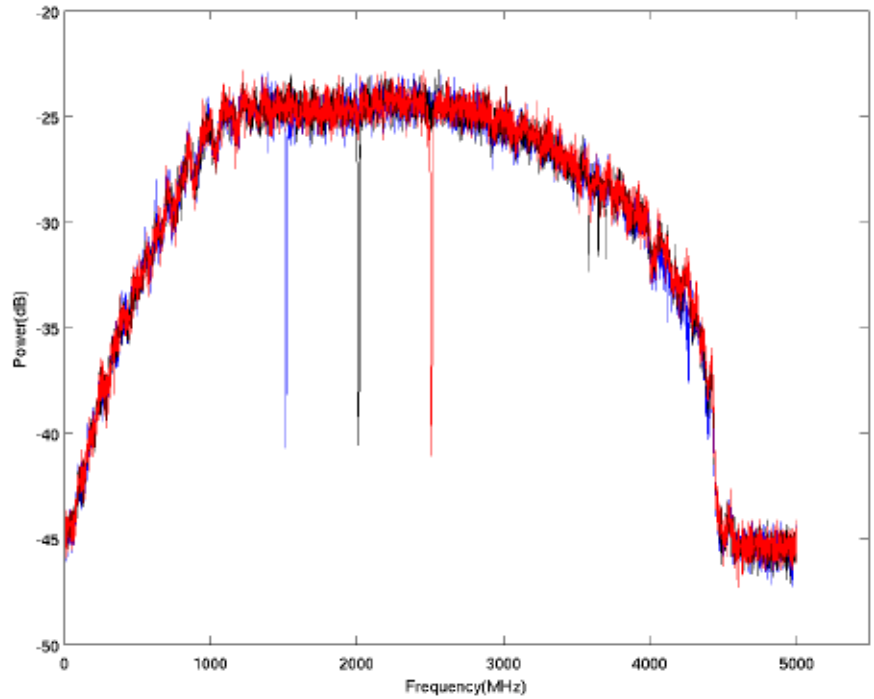
A 10 GSa/s single core CASPER ADC

based on Adsantec ANST7120A-KMA

Jiang, Yu & Guzzino (2016)

Homin Jiang, ASIAA, with 10 Gsps ADC



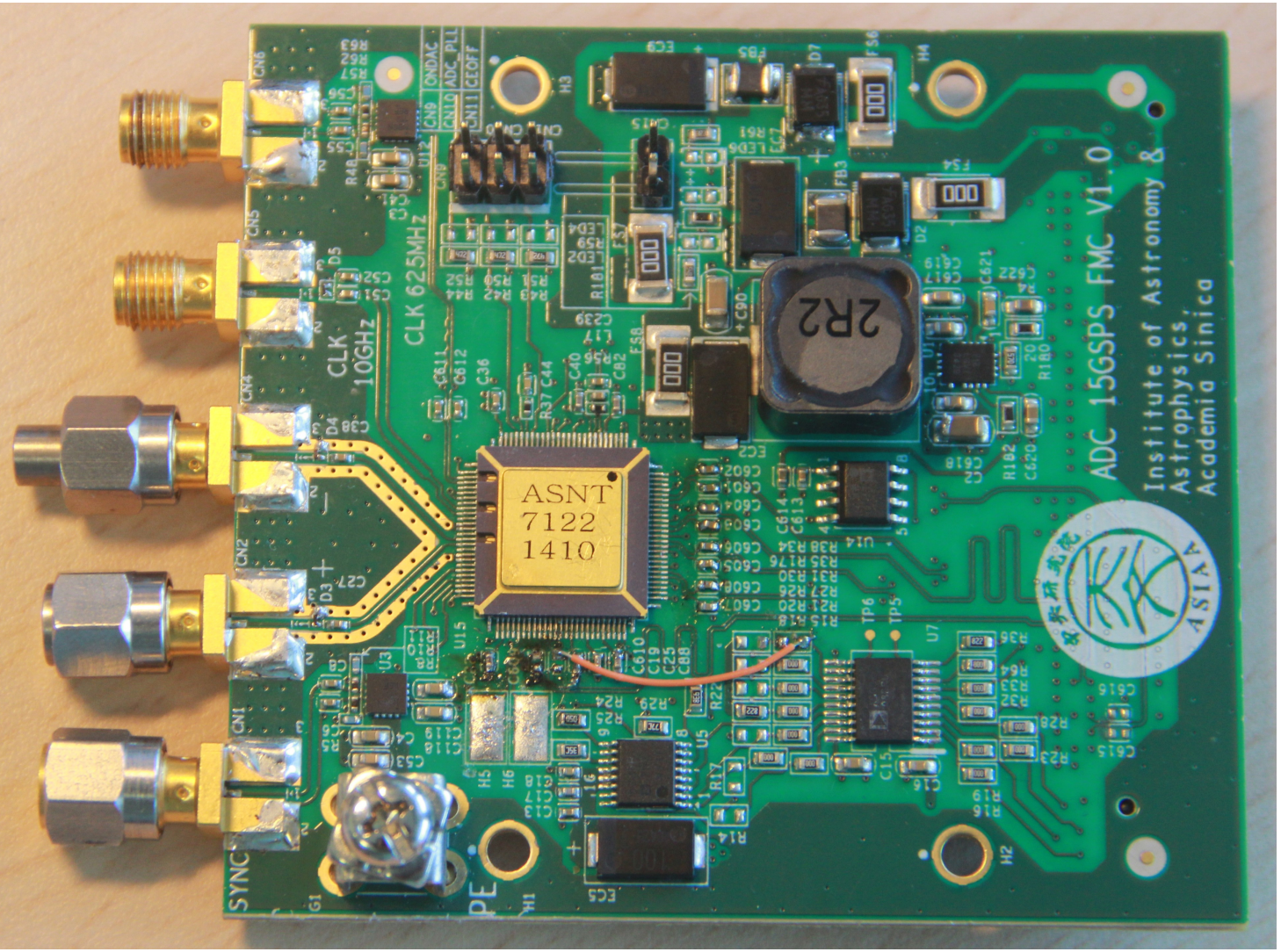


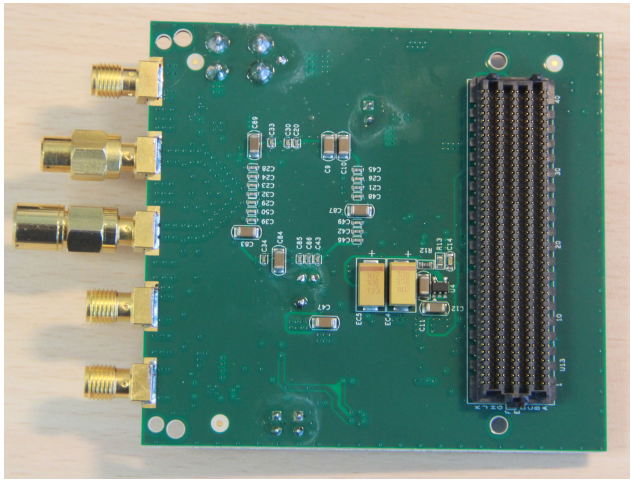
Analog frequency response 0 to 5 GHz

A 16 GSa/s single core CASPER ADC from ASIAA

based on Adsantec ANST7123A-KMA

Jiang, Yu, Chen & Liu (2018)





Digital Interface is SERDES on FMC+

Photos courtesy Homin Jiang, ASIAA

8 GHz bandwidth sampled at 4-bits produces data rate of 64 Gbps (fits comfortably on 100 Gbps Ethernet Link)

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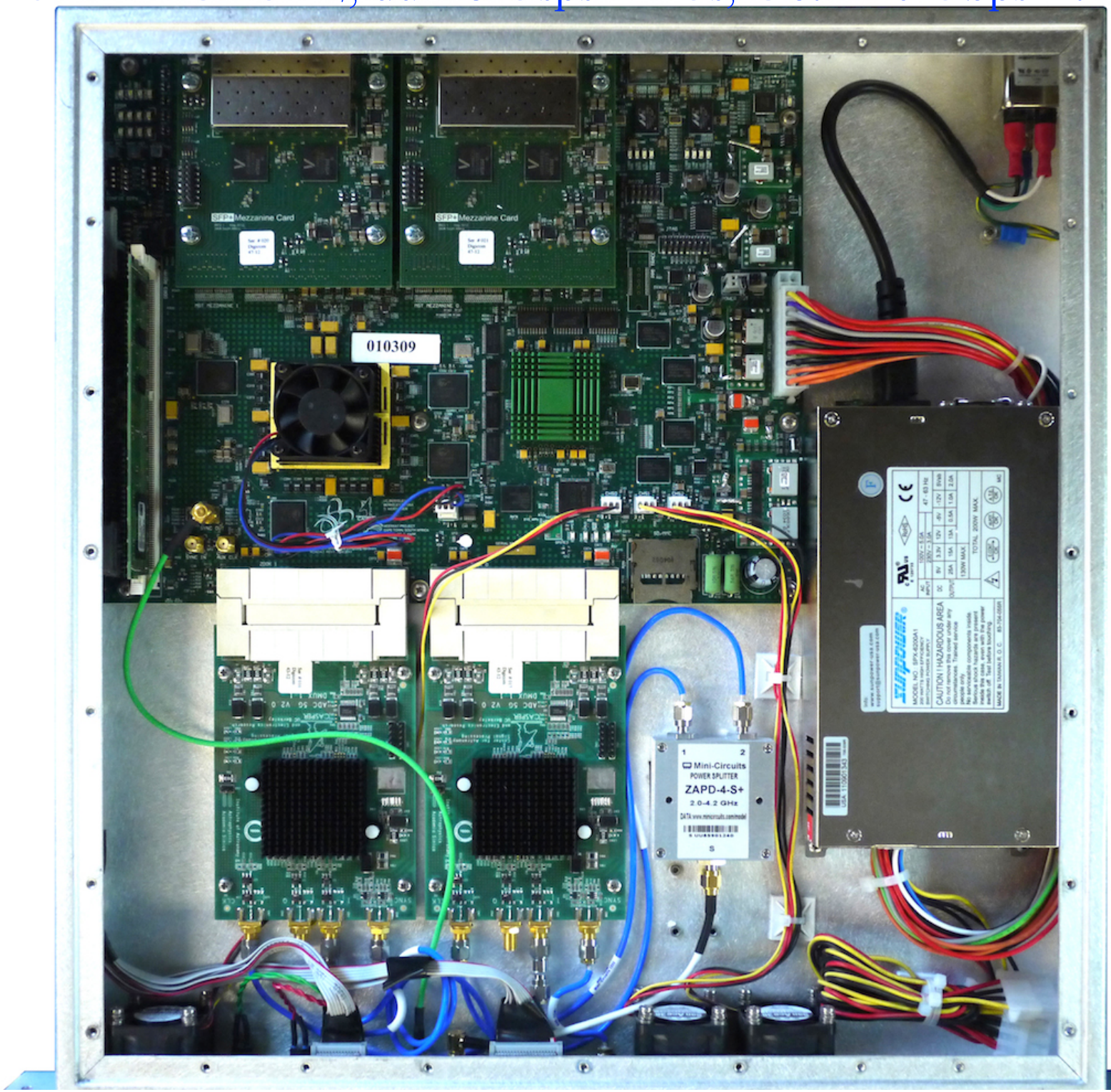
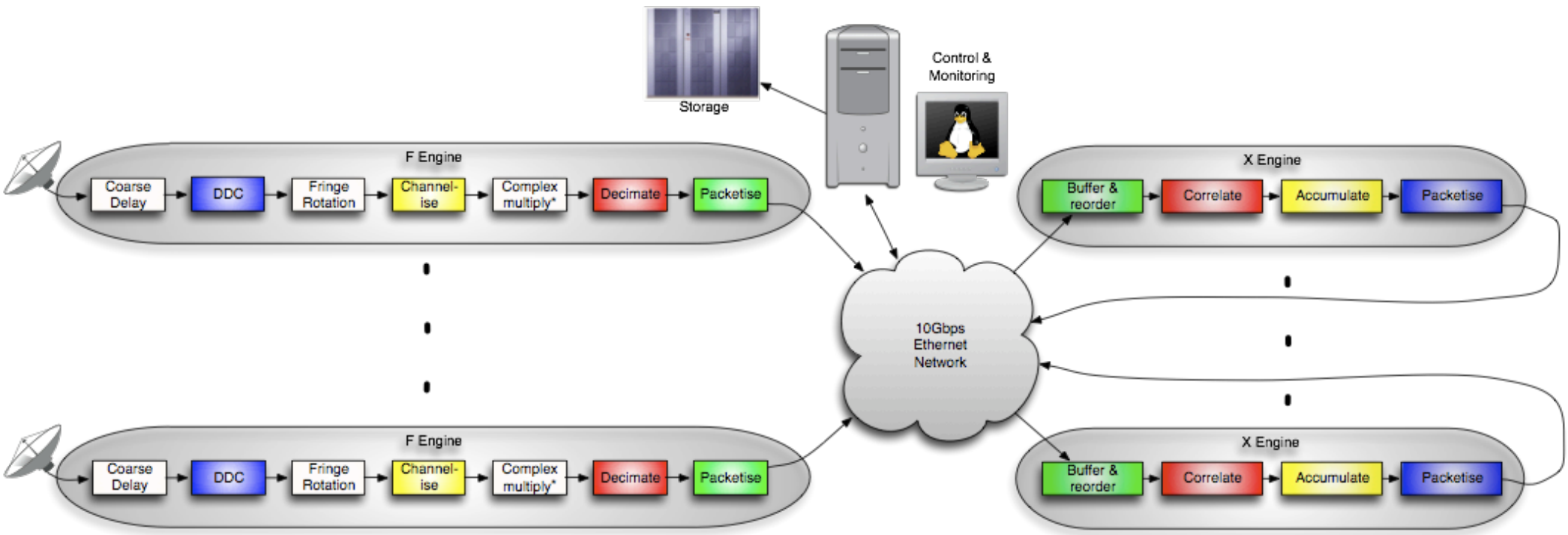
CASPER ROACH2, dual 5 Gsps ADCs, Octal 10 Gbps Ethernet



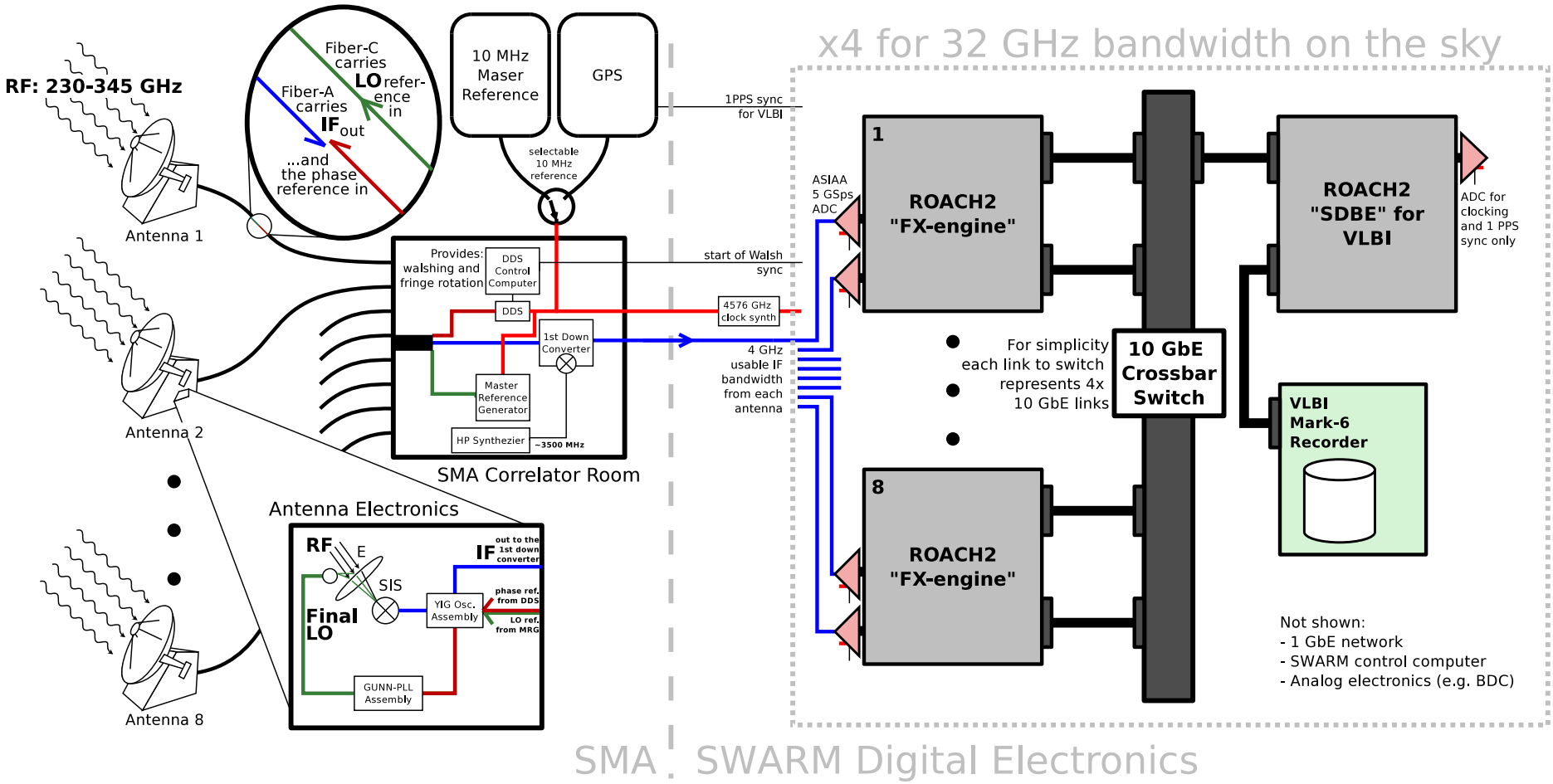
CASPER Correlator Concept



*Complex multiply allows for fine delay control and per-channel digital gain control.
White coloured blocks not yet implemented.

SWARM: SMA Wideband Astronomical ROACH2 Machine

(Primiani et al., JAI, V5 (4) 2016)



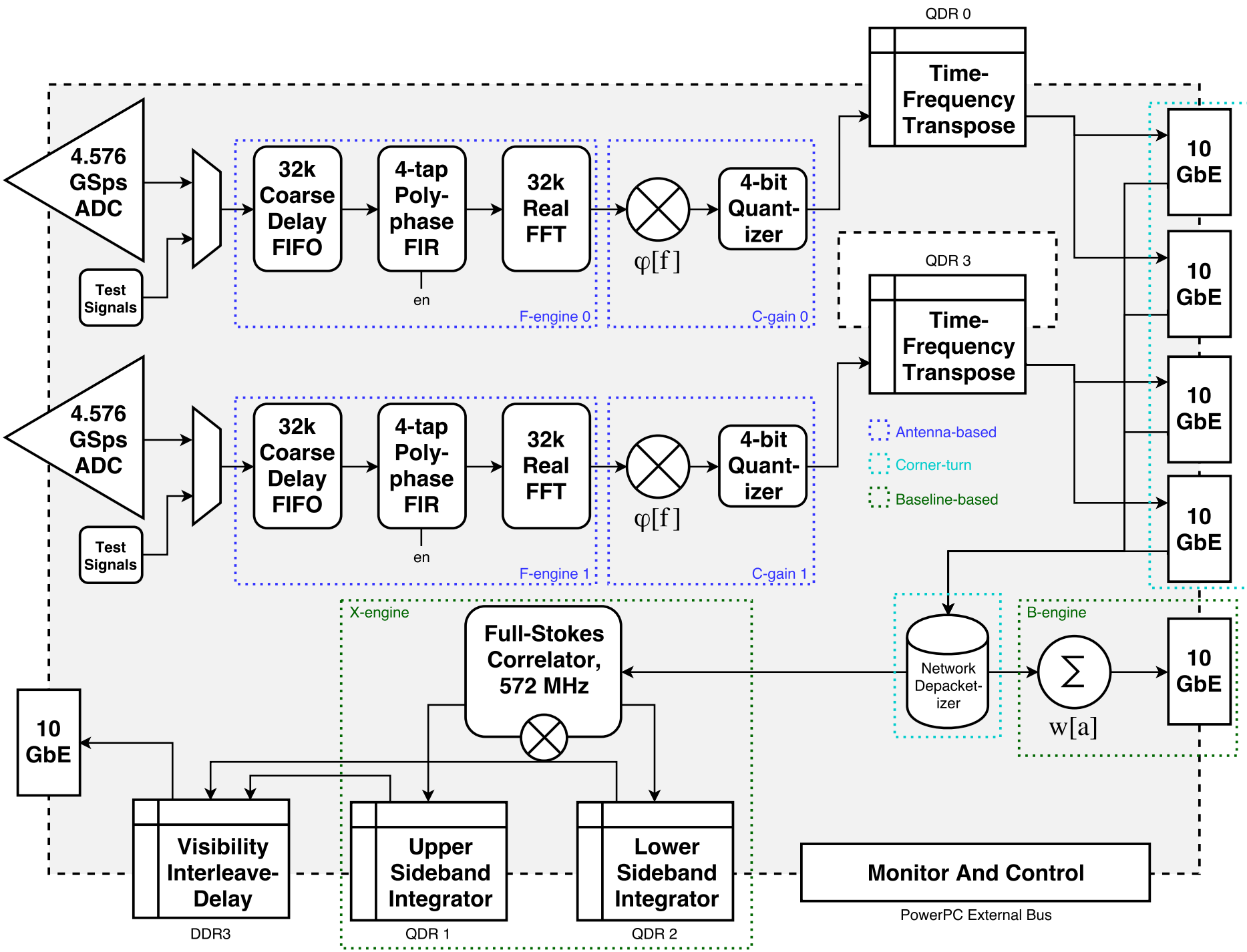
1 "quadrant": 2 GHz per receiver per sideband = 8 GHz; 32 GHz total

Benefits relative to ASIC correlator:

1. high uniform spectral resolution with no sacrifice of bandwidth,
2. smaller footprint and power consumption.
3. better digital efficiency with 4-bit cross-correlation
4. 2 GHz wide bands easier to reduce, result in higher quality spectra
5. Natively supports VLBI phasing and recording, 16 Gbps/quadrant
6. Built with CASPER and COTS components

SWARM FPGA logic subsumes great complexity, fits in single Virtex 6 SX475T

(Primiani et al., JAI, V5 (4) 2016)



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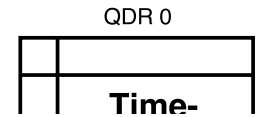
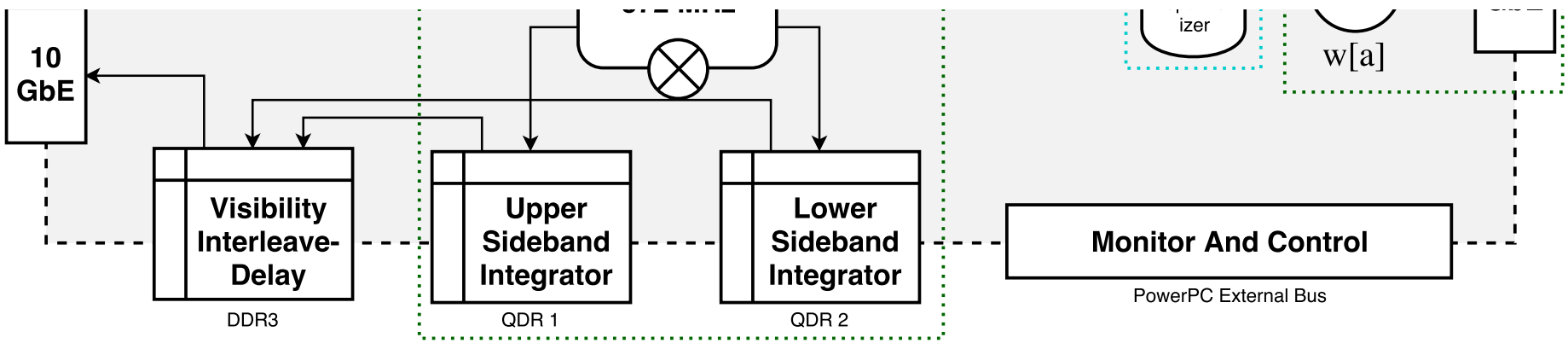


Table 2. Resources used by various subsystems of the SWARM gateware.

	DSP Slices	Slice LUTs	Slice Reg.	Block RAM	Slices
Available[a]	2,016	297,600	595,200	1,064	74,400
F-engine 0	336 (16.7%)	66546 (22.4%)	74637 (12.5%)	232 (21.8%)	21059 (28.3%)
F-engine 1	336 (16.7%)	66756 (22.4%)	74637 (12.5%)	232 (21.8%)	20700 (27.8%)
Complex gain 0	64 (3.2%)	3929 (1.3%)	3640 (0.6%)	64 (6.0%)	1876 (2.5%)
Complex gain 1	64 (3.2%)	3909 (1.3%)	3641 (0.6%)	64 (6.0%)	1640 (2.2%)
X-engine	4 (0.2%)	44475 (14.9%)	47244 (7.9%)	95 (8.9%)	10394 (14.0%)
B-engine	42 (2.1%)	1646 (0.6%)	2101 (0.4%)	10 (0.9%)	868 (1.2%)
Other	64 (3.2%)	55297 (18.6%)	58479 (9.8%)	200 (18.8%)	16988 (22.8%)
Total	910 (45.1%)	242558 (81.5%)	264379 (44.4%)	897 (84.3%)	73525 (98.8%)

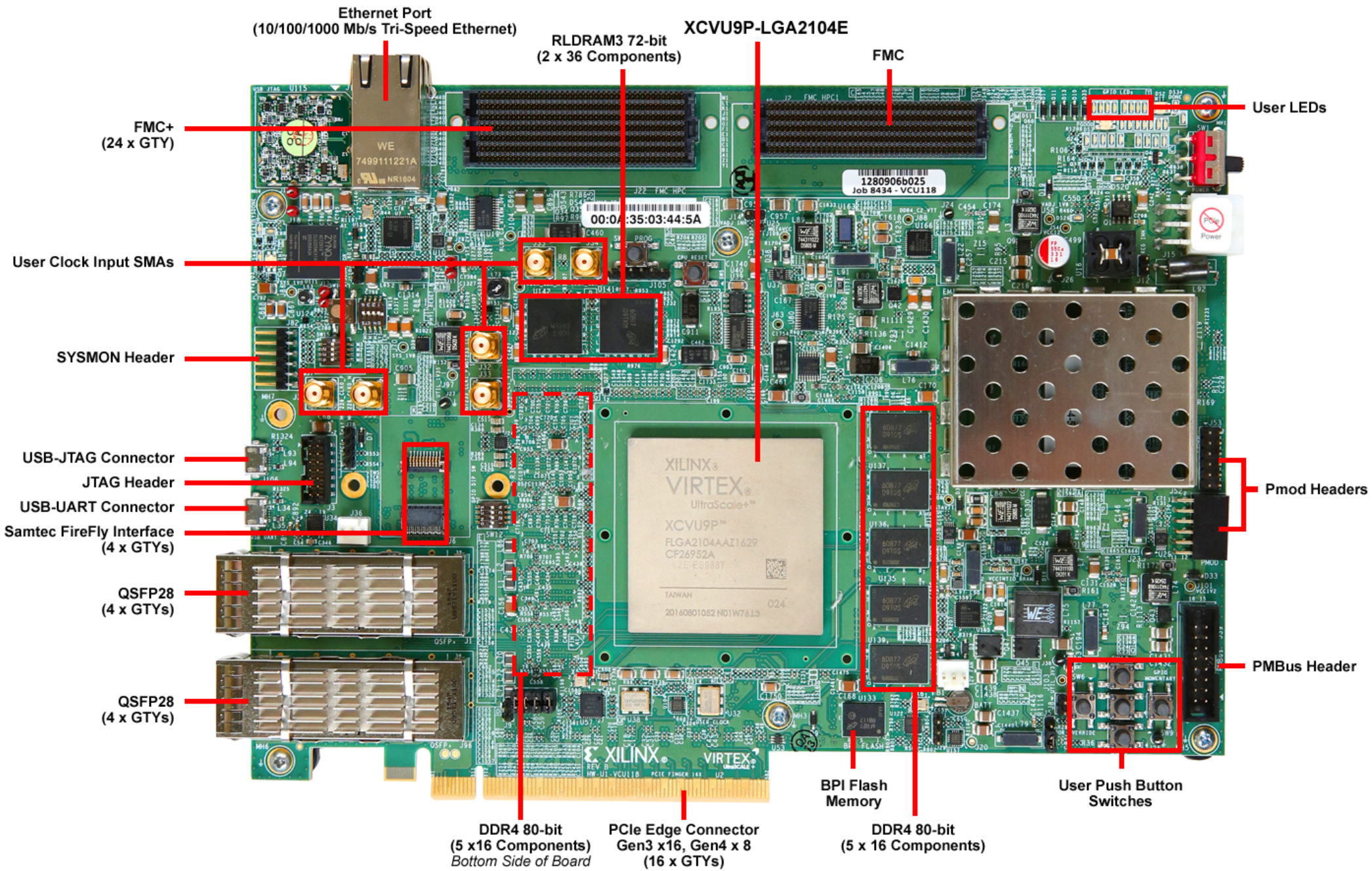
Note: [a]Shown for the Xilinx Virtex-6 SX475T.

Also: FPGA Fabric Clock 286 MHz



VCU118 COTS hardware, $6,995 each

(Ultrascale+ VU9P FPGA)



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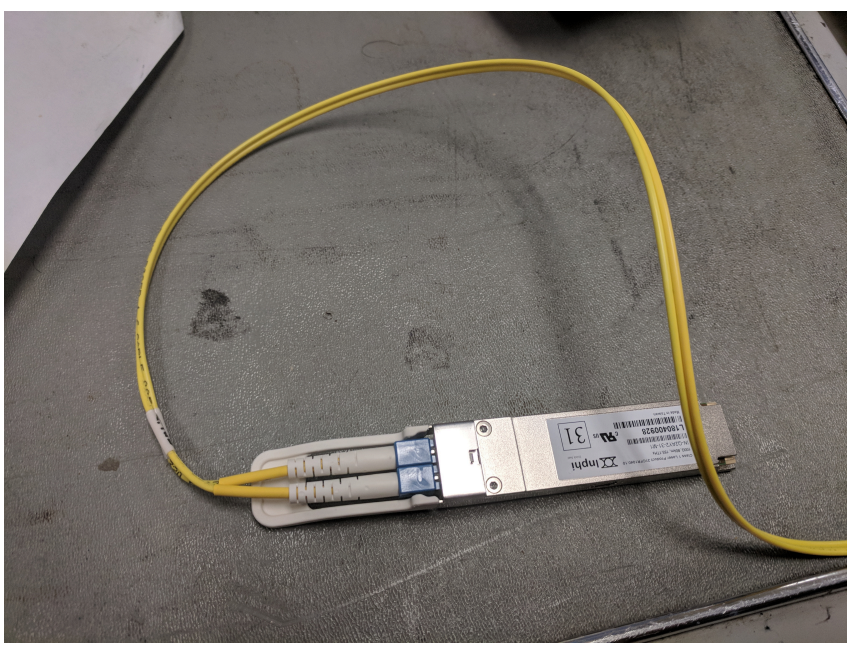
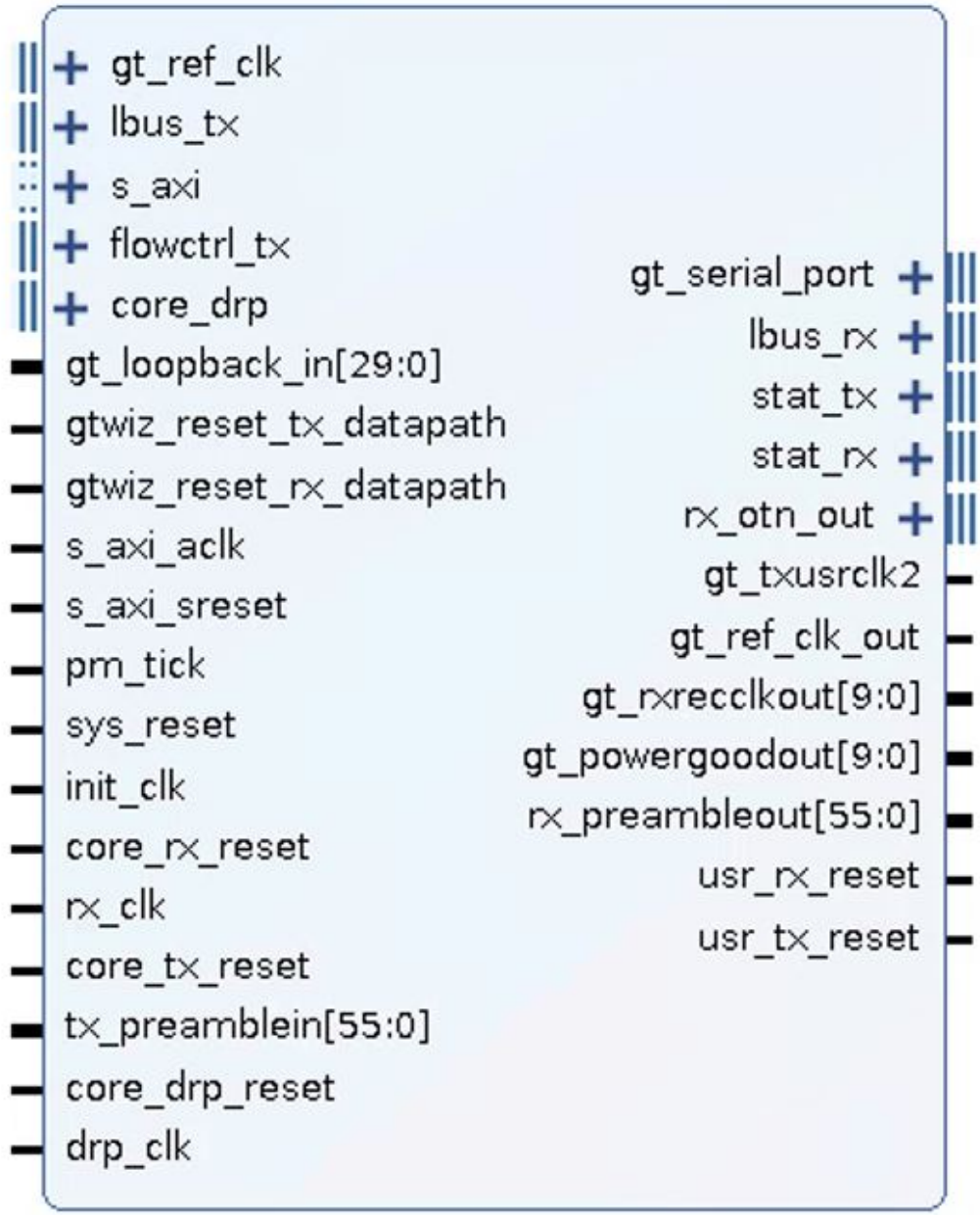
100 Gbps Ethernet Developments

current, with A. Roshanineshat, R Wilson, J. Test

copper



Fiber

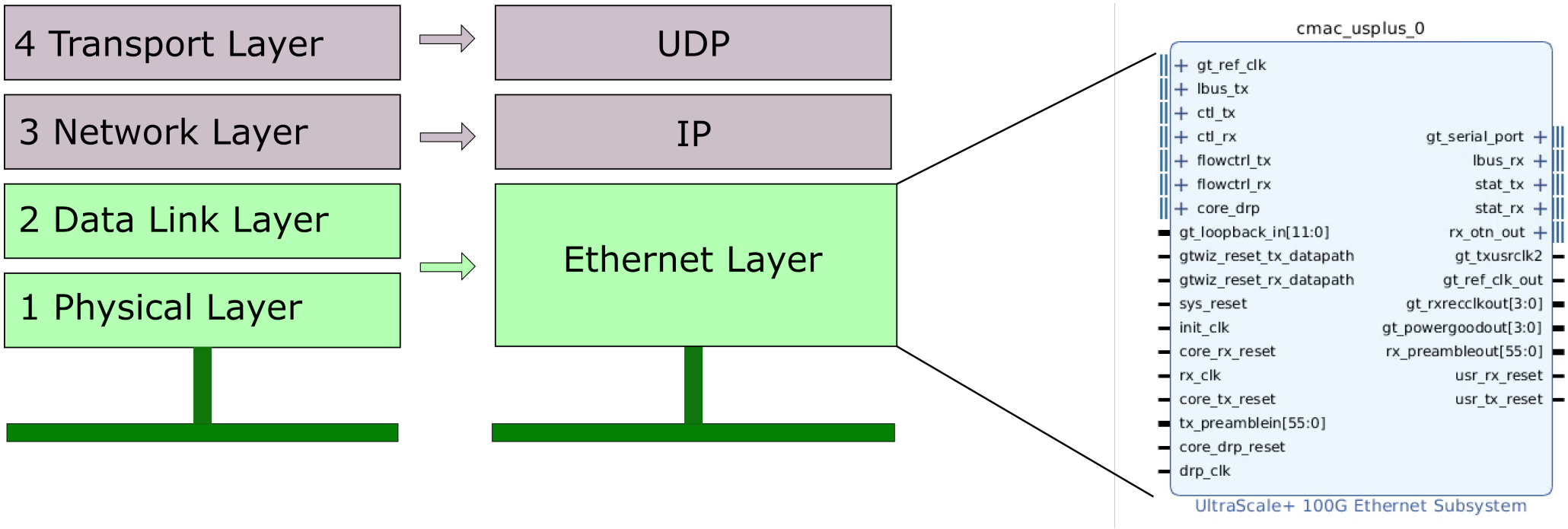


Ultrascale+ IP Core and Stack

(provided by Xilinx in Vivado)

SAO Open Source Ethernet Protocol Stack

Arash Roshanineshat, 2018



- Based on Open Systems Interconnect (OSI) model
- Xilinx-supplied Ultrascale+ 100G Ethernet IP core only supports to Ethernet: layer 2 of OSI
- IP and UDP layers implemented on VCU118 in lab using Verilog and Vivado
- Data is wrapped by UDP, IPv4 and Ethernet frames in order and then is transmitted.

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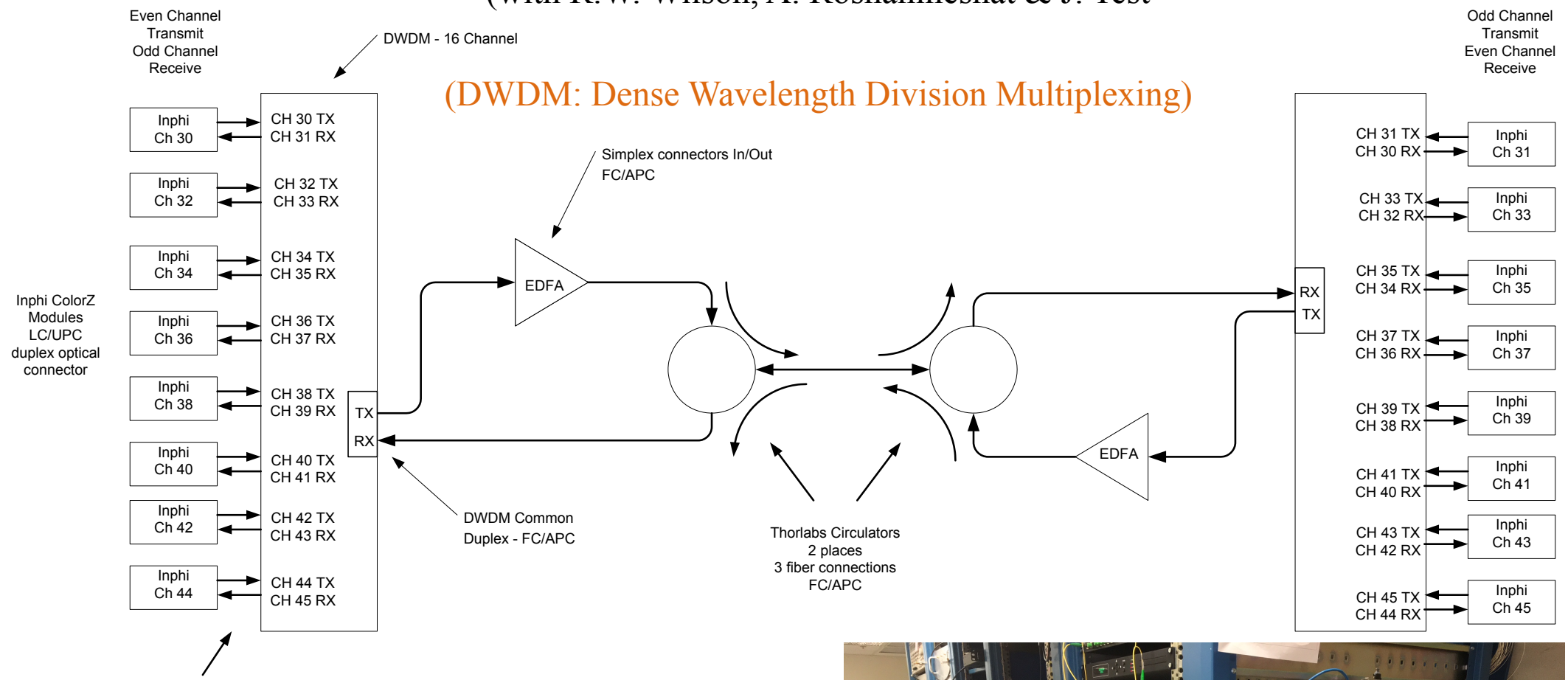
100 Gbps full duplex DWDM Ethernet on single fiber

(128 GHz bandwidth wSMA would require 8 100Gbps DWDM links per antenna)

(with R.W. Wilson, A. Roshanineshat & J. Test



Color-Z DWDM modules from Inphi

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Potential benefits beyond SMA

ALMA Memo 607

SAO Cycle 3 Development Study Closeout Report

Digital Correlator and Phased Array Architectures for Upgrading ALMA

Alain Baudry, Lindy Blackburn, Brent Carlson, Geoff Crew, Shep Doeleman,
Ray Escoffier, Lincoln Greenhill, Daniel Herrera, Jack Hickish, Rich Lacasse, Rurik Primiani,
Michael Rupen, Alejandro Saez, Jonathan Weintroub (PI) & André Young

December 22, 2017

Abstract

This Closeout Report documents the outcome of a SAO-led ALMA Development Study of a next generation combined correlator and VLBI phased array to take greater advantage of fundamental scientific capabilities, such as sensitivity, resolution and flexibility. ALMA already represents a huge advance in collecting area and frequency coverage making it the dominant instrument for high frequency radio astronomy. We have studied processing architectures that maximize bandwidth, and thus sensitivity, allow flexible ultra high resolution spectral processing, and supports other operational modes, such as VLBI. The ALMA Science Advisory Committee (ASAC) studies *Pathways to Developing ALMA* and *A Road Map for Developing ALMA* (both referenced as Bolatto et al., 2015) comprehensively describe the community view of ALMA upgrades and their key science impact.

The methodology of the Study was to examine a variety of technologies, algorithms, balancing costs and timelines against potential benefits. The scientific impact for the proposed study derives from several key new areas of enhanced capability. The Study is divided into eight technical work packages. This Outcomes Report gives a concise summary of each, and eight detailed appendices are provided. A top-level conceptual framing of the full installation, including specifications and rough equipment costing and schedule, is presented as Phase III of three suggested design phases. Phase I is this Study, now complete.

Figure 1 Study team group photo under the CHIME array taken at the Study closing meeting , NRC-Herzberg, Penticton, BC, Canada, 24 February 2017

ALMA Memo 607

SAO Cycle 3 Development Study Closeout Report

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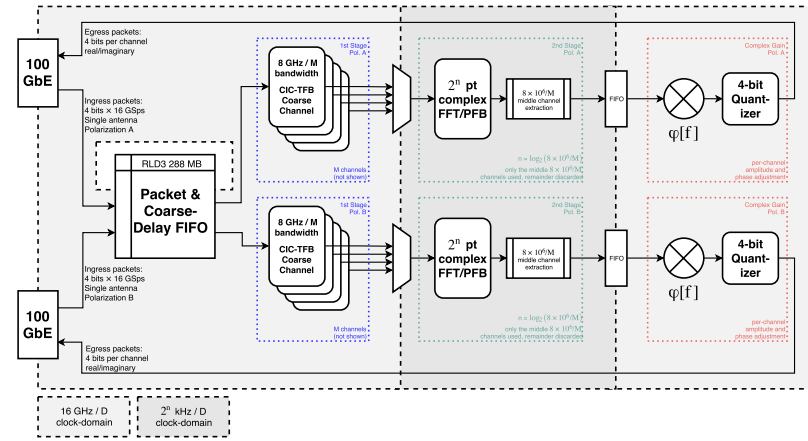


xGPU [Clark et al, 2012]

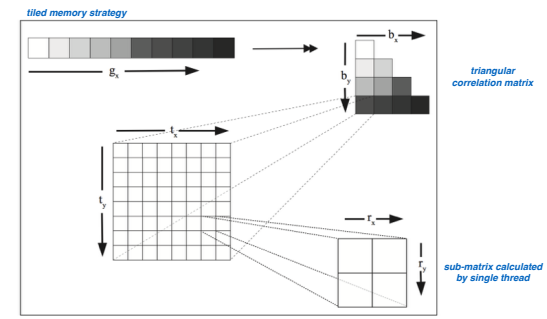
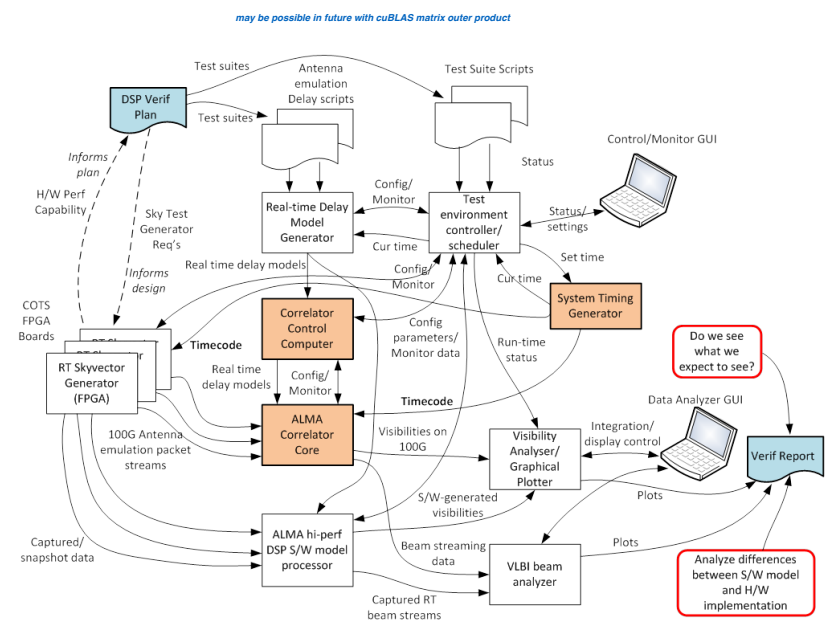


Figure 3: Schematic description of the how threads are mapped to the correlation matrix. The linear grid index g_x is mapped to the triangular block index (b_x, b_y). Each thread (t_x, t_y) within the thread block is then responsible for calculating an $R_x \times R_y$ tile of the correlation matrix (indexed by (r_x, r_y)). The grid index g_y maps trivially to the frequency dimension (not shown).



wSMA technology applied to ALMA

- International ALMA study team have developed a ultra-wideband correlator/phased array design concept, using *proven (at SMA)* packetized FX technology
- Concept is a powerful, flexible and transformative upgrade
- Four times BW, 1kHz resolution, phased array and 4-bit math for 99% efficiency, native VLBI capability
- It fully supports the ALMA2030 science vision
- The concept has a number of benefits including:
  - Scalable and extensible (e.g. to array feeds), flexible and supports user instruments
  - Small, and it can be assembled while present operational system is running
  - Native phased array, with very low latency in phase-feedback look for efficiency
  - 4-bit arithmetic in all modes translates to an effective 22% time savings (80 days/year)
- If started now, we could produce a fully commissioned upgrade by ~2028 at modest cost (materials ~$10M)

ALMA Memo 612

ALMA BOARD

ALMA EDM Document	AEDM 2018-017-O
Distribution	**Ordinary Session**

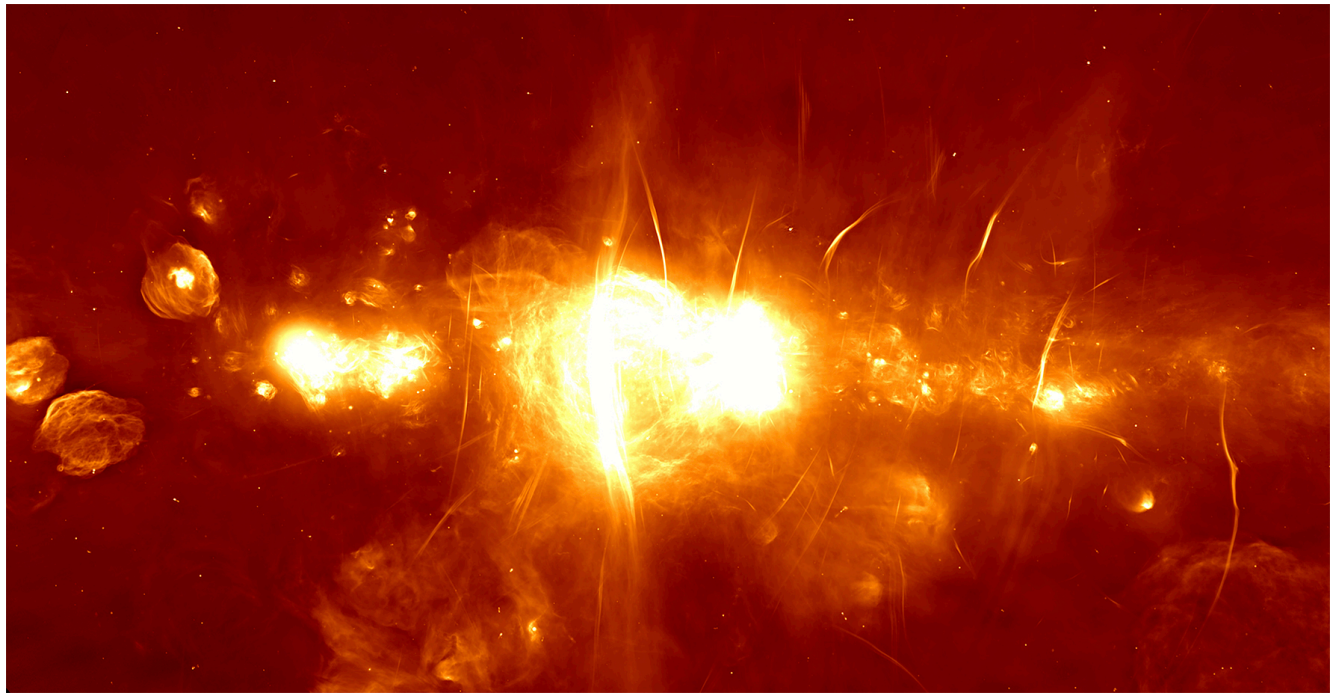
Subject: The ALMA Development Roadmap

Authors: J. Carpenter, D. Iono, L. Testi, N. Whyborn, A. Wootten, N. Evans
(The ALMA Development Working Group)

Sidebar: MeerKAT; Multicast: data products by subscription

Manley et al. 2018

- MeerKAT dedicated 13 July.
- All data products available in network by subscription.
- Supports user instruments (USE).
- Commensal USE includes GPU-based frequency-domain beamformers, transient search detection hardware, SETI and pulsar timers.



The best way to predict the future is to create it

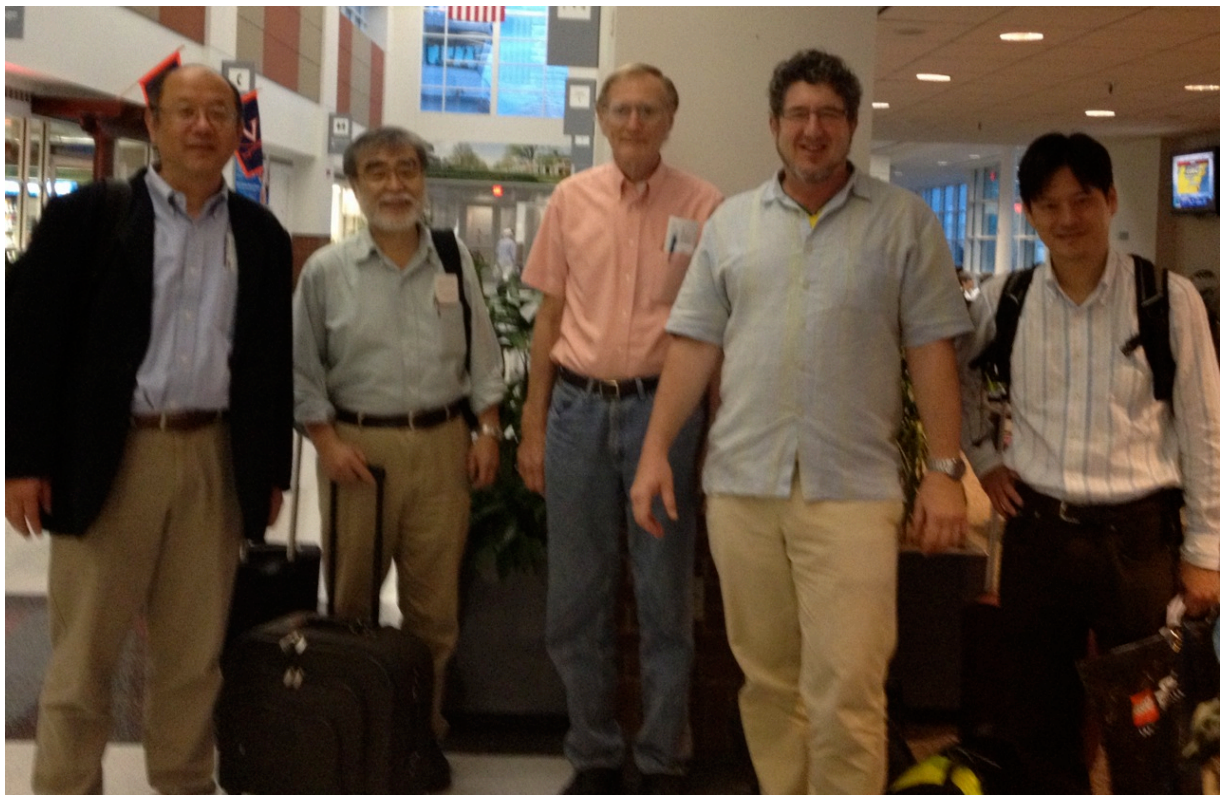
Abraham Lincoln

- 32 GHz SWARM, a CASPER facility deployment in 2017, has transformed operations at SMA
- Engineering decisions made at SWARM's inception validated:
  - Quad-Core wideband ADC technology for science-quality data
  - Fit in FPGA a hi-res FX correlator with EHT phasing and recording
  - ROACH2 platform and 5 GS/s ADC now a mainstay of EHT
- wSMA 128 GHz bandwidth needs cutting-edge tech
  - 16 Gsps Adsantec ADC
  - Ultrascale+ FPGA
  - 100Gbps Ethernet & DWDM
- wSMA future is bright:
  - Develop and access yet wider band ADC, FPGA DSP and100 Gbps
  - Transform SMA with a four-folding of bandwidth.
  - Apply wSMA technology to upgrade ALMA

Questions?

"With correlator performance having gone up by a factor of 922,000 over the last 30 years, its only fair that correlator design engineers' salaries should have gone up by a similar factor"

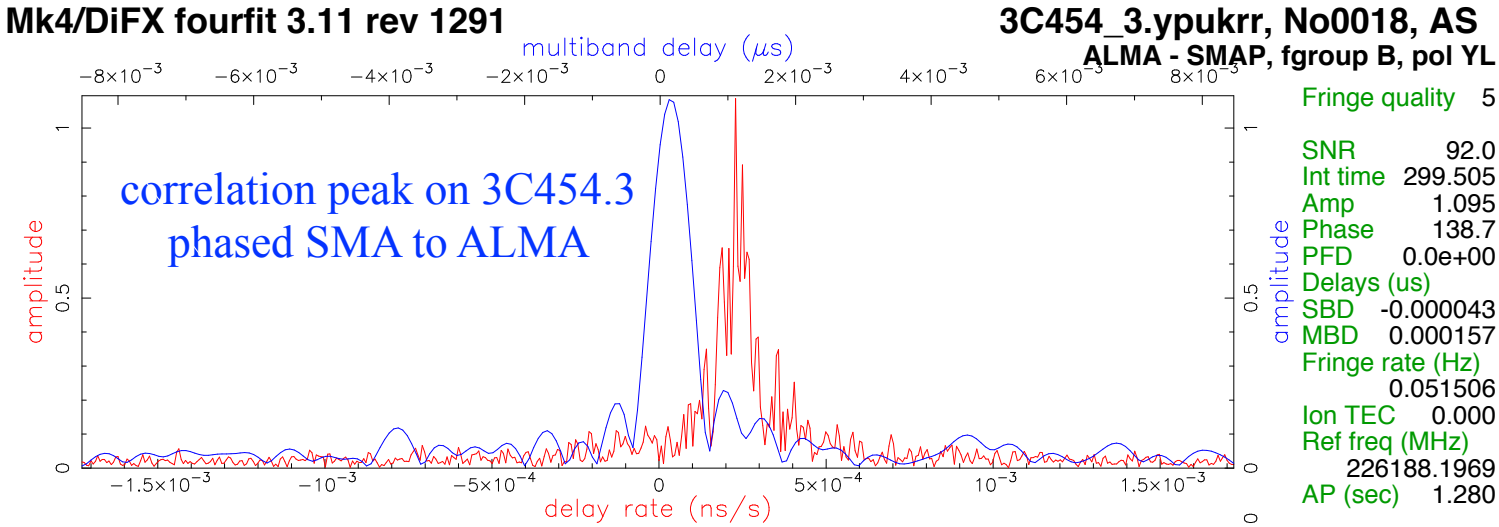
Ray Escoffier, leader of N.A. ALMA correlator team, over a decade ago



SWARM is Event Horizon Telescope ready

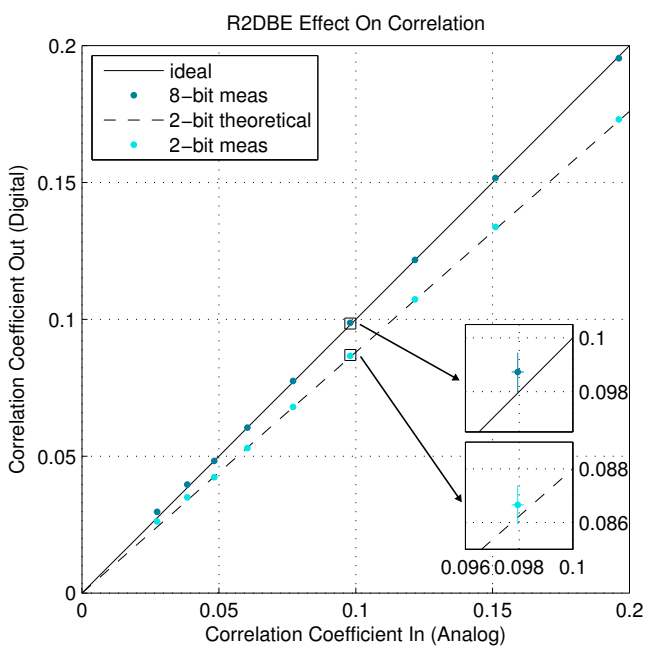
Phased ALMA to SMA Fringe, 22 Jan 2016

2015, 2016, 2017 annual campaigns observed and fringes verified. 2017 spectacular weather, excellent data set.



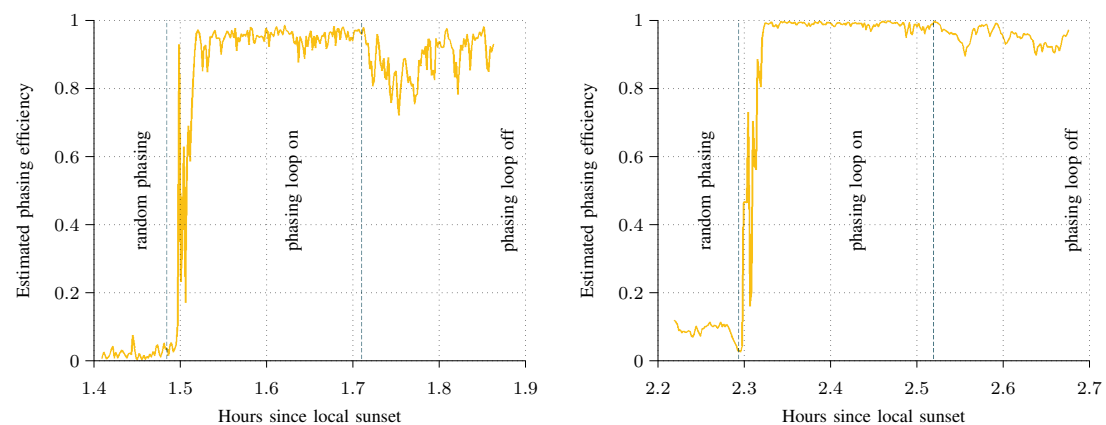
Geoff Crew, Mike Tttus, Roger Cappallo, Adam Deller, ALMA phasing Geoff Crew and Lynn Matthews, and many more!

Single dish digital back end based on ROACH2 also



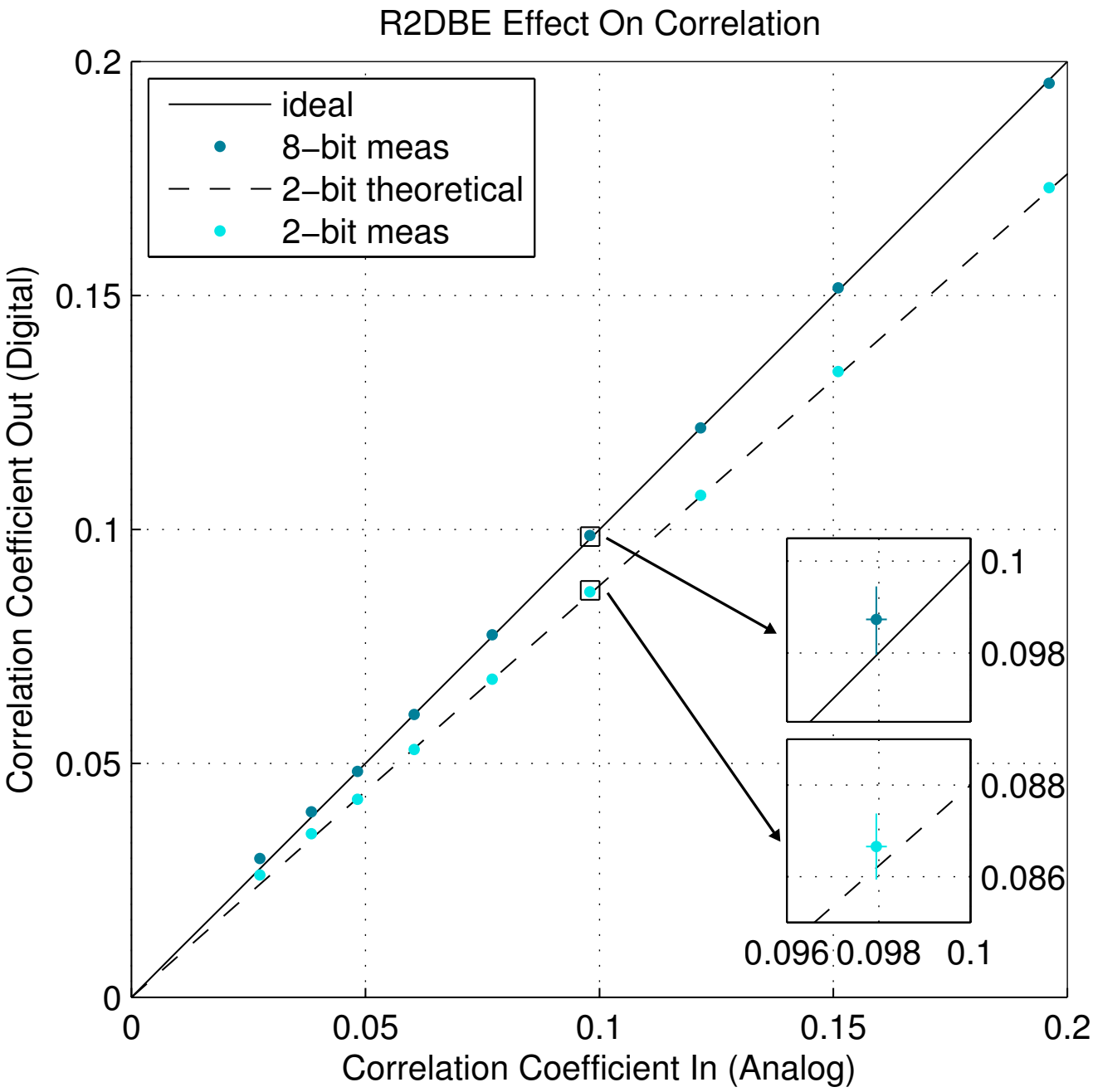
Laura Vertatschitsch et al, PASP, (127) 958, 2015

SMA phasing efficiency test



A. Young, Primiani, K. Young, Weintroub, et al., IEEE Phased Array Conference, October 2016

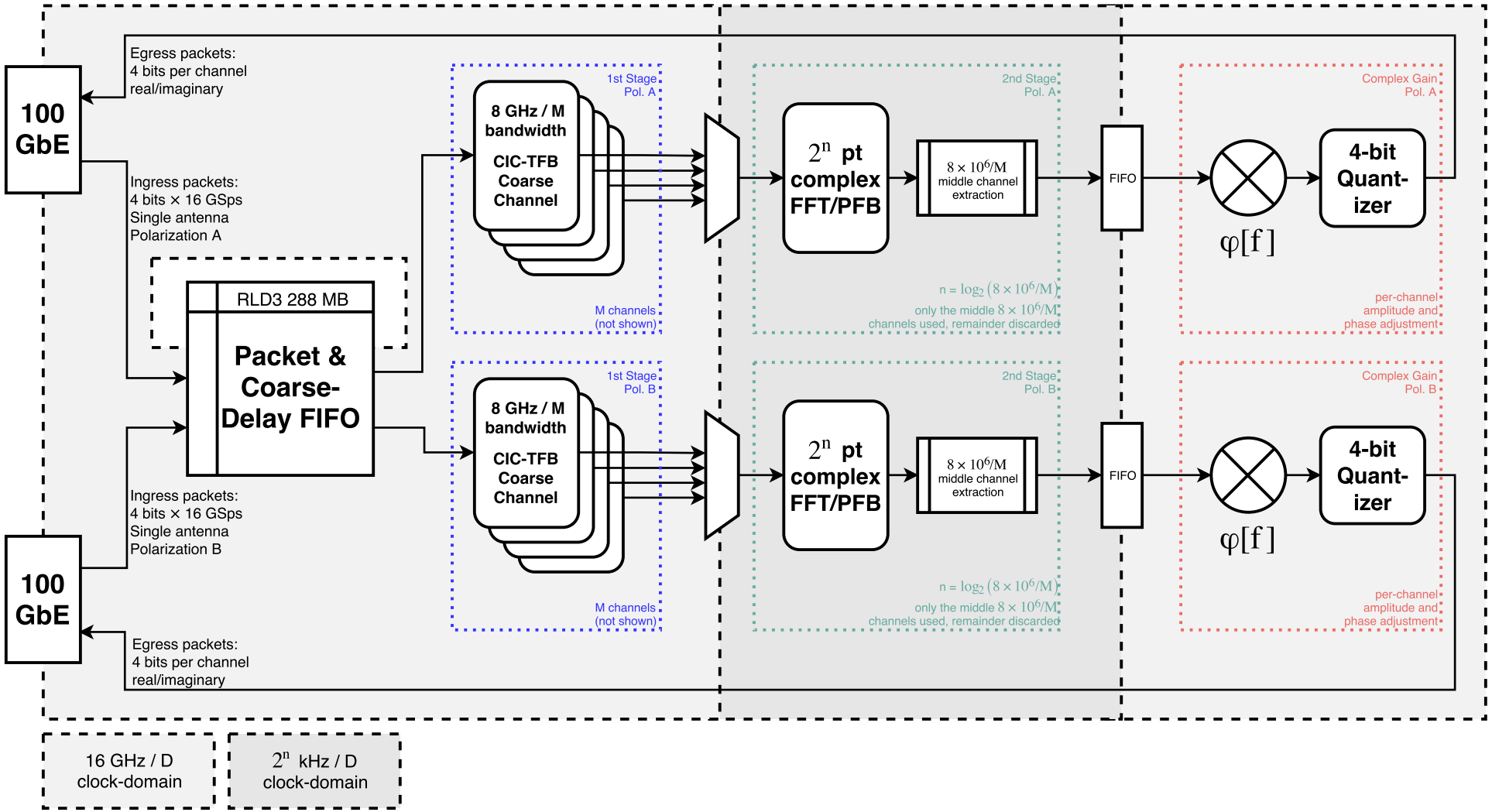
Single dish 8 Gbps digital back end based on ROACH2



Laura Vertatschitsch et al, PASP, (127) 958, 2015

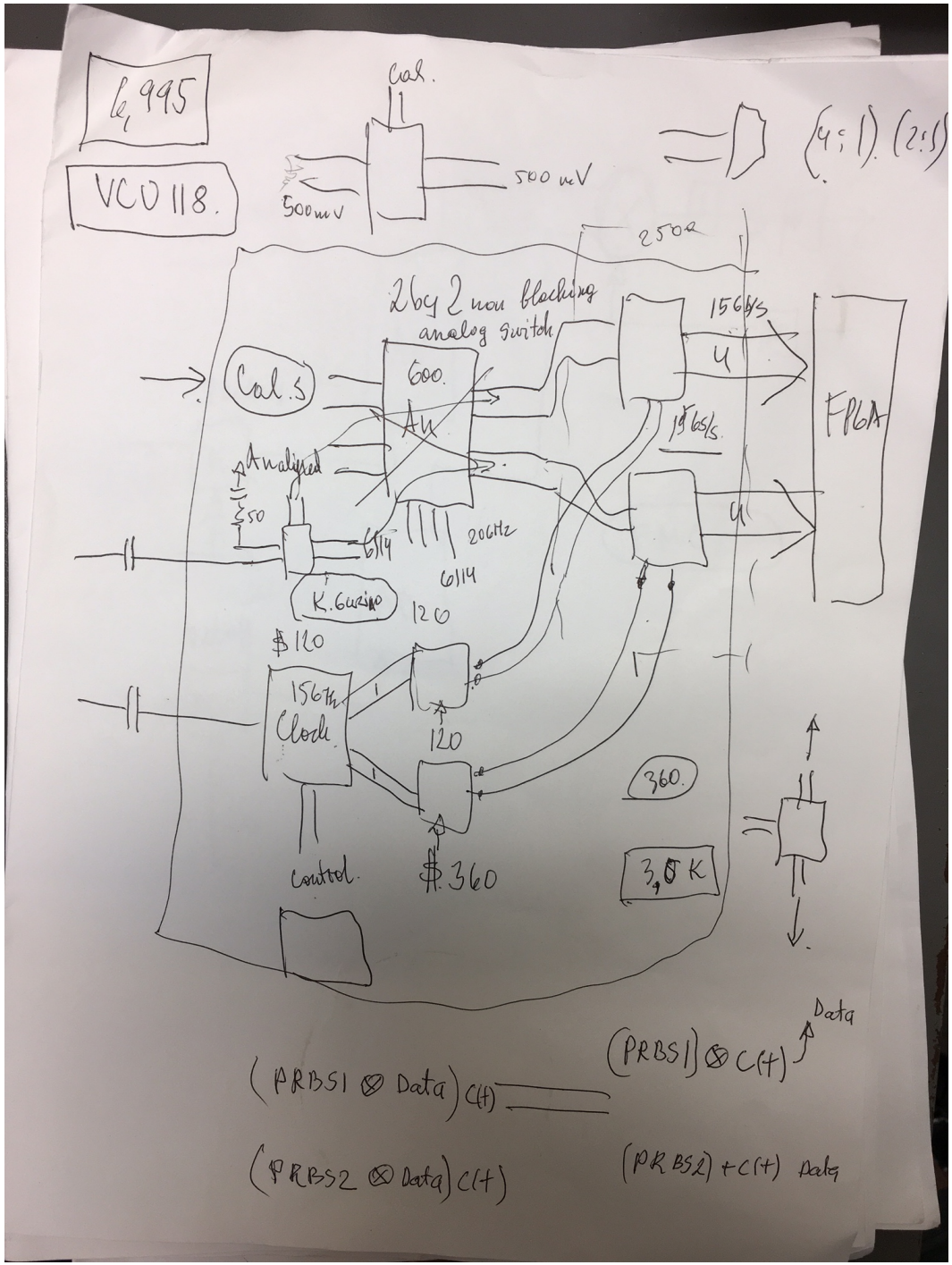
First setup built for South Pole 2014

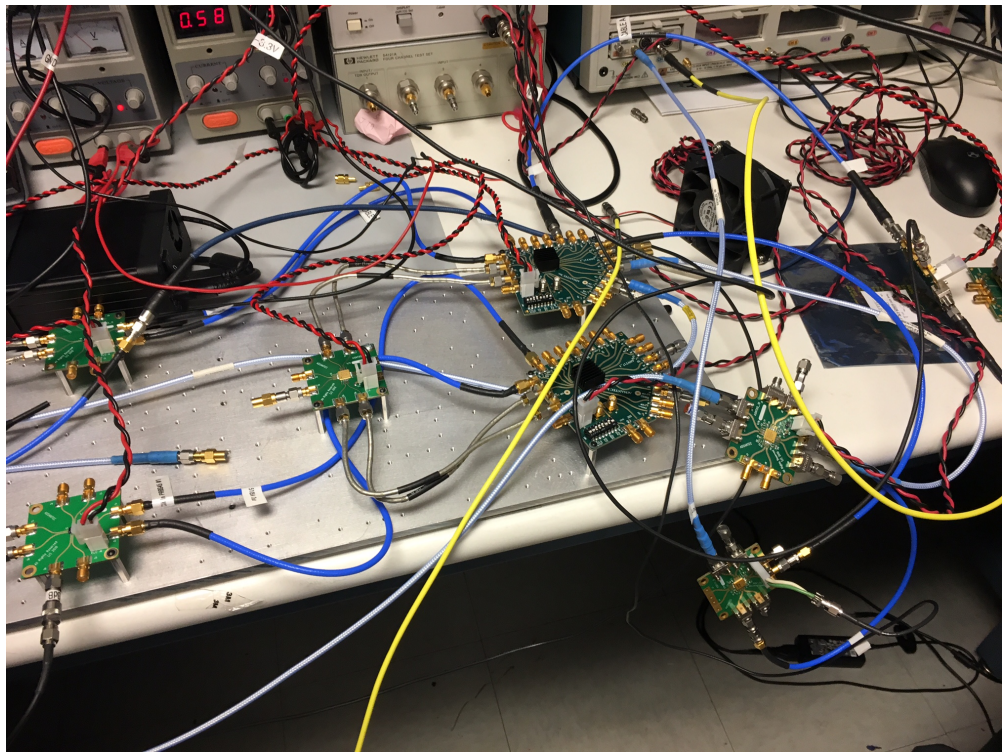
One way to get 8 GHz blocks with 1kHz resolution

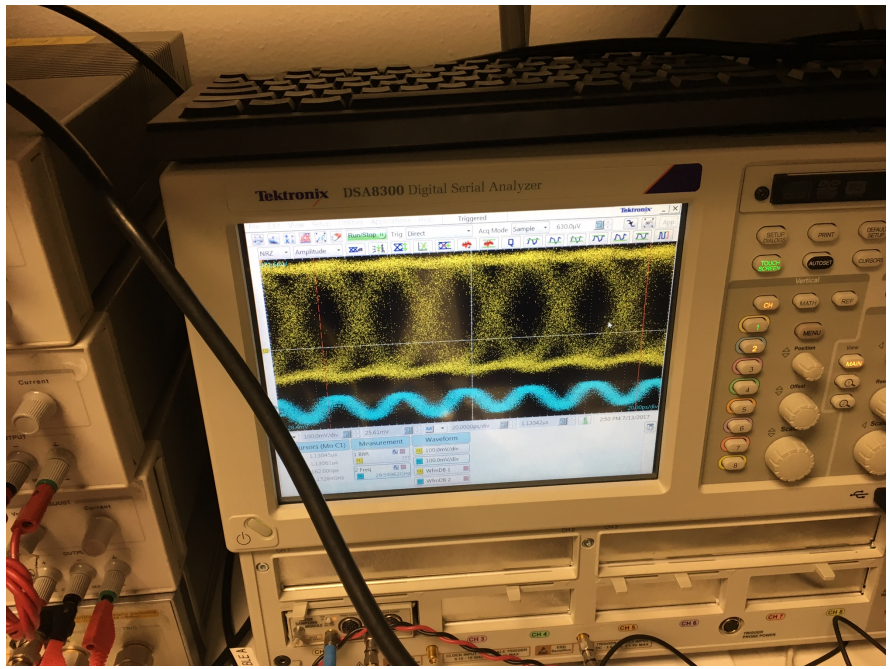


Candidate ALMA F-engine gateware fits XCV9P or XCV13P

Dual interleaved Adsantec ASNT7122 30 GS/s







Item	Quantity	Cost each	Power each	Cost total	Power total
VCU118 VU9P FPGA	8	$6995	125W	$55,960	1 kW
PCIe Server for FPGA	4	$4,200	150W	$16,800	0.6kW
Switch	1	$44,998	500W	$44,998	0.5 kW
GPU Server	4	$18,800	370W	$75,200	1.5 kW
network cables	52	$450	0W	$23,400	0
totals				**$216,358**	**3.6 kW**

Table excludes emulator and cooling

To outfit ALMA requires a 36-folding

130 kW and about $7.8M—equipment only

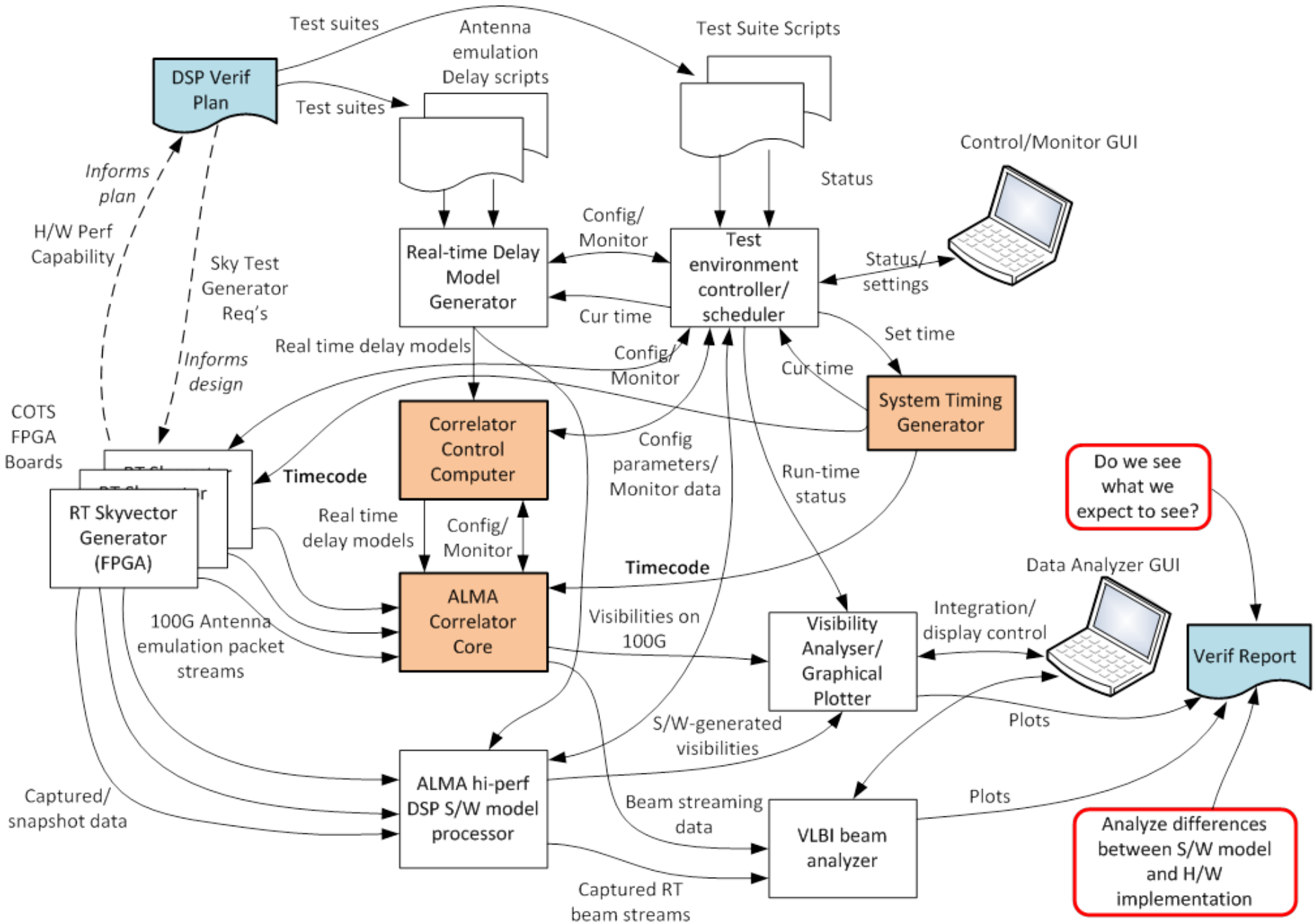
Very recent news: Project Proposal declined. ngALMA SysEng needed

Ultrascale+ (chip and board) pricing data summary

Part #	Vendor	Cost	Comments
VCU118 (XCVU9PL2FLGA2104)	Xilinx/Avnet	$6995	
XCVU9P-1FLGC2104E	Avnet	$27k	
XCVU9P-2FLGB2104E	Digikey	$43k	
XCVU13P-2FLGA2577I	Avnet Europe	EUR71k	
HTG-910 HTG-VUSP-PCIE-9P	Hitech Global	$30k	Pricing to JH in Feb $10k
HTG910 HTG-VUSP-PCIE-13P	Hitech Global	$36k	…$15k

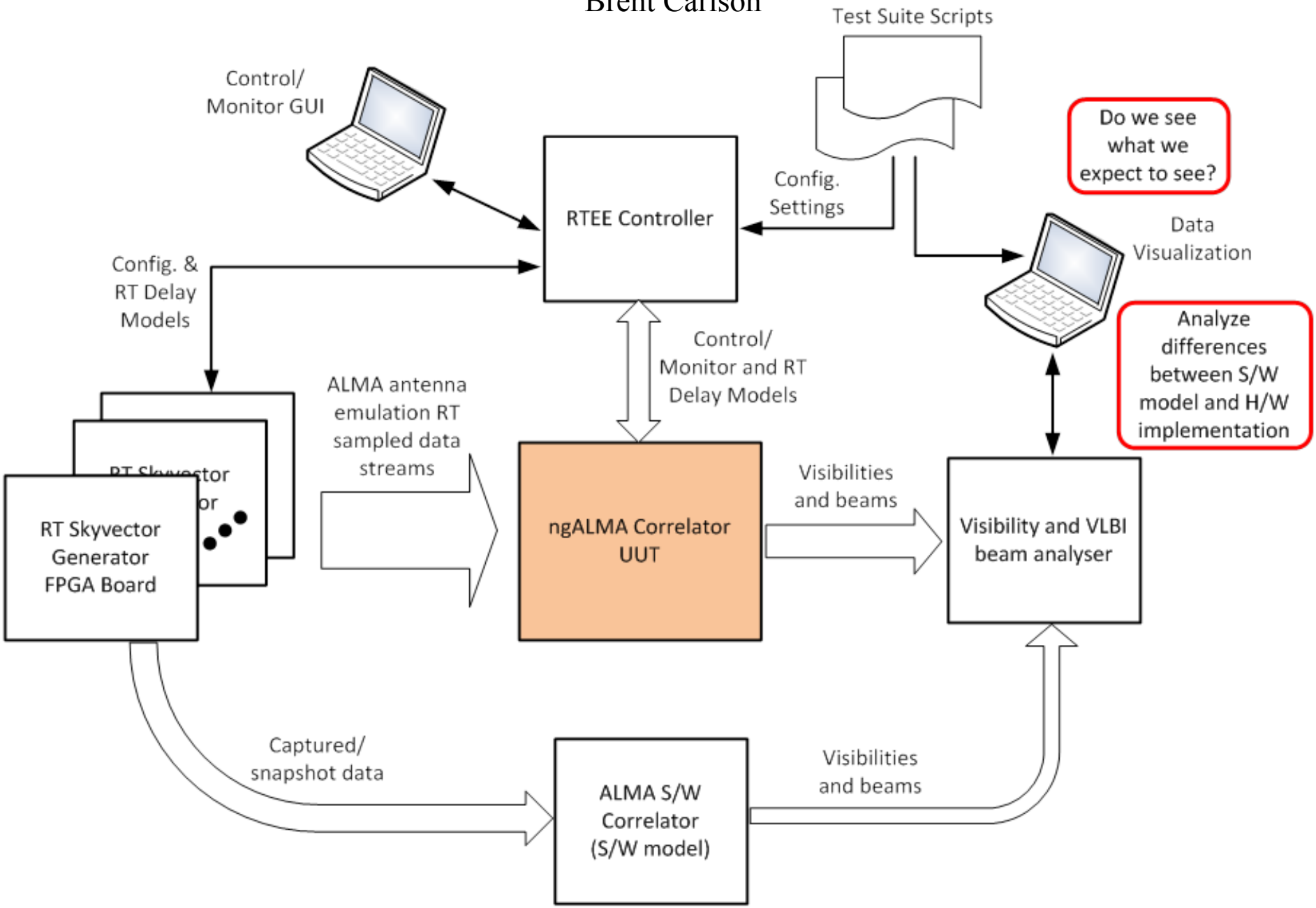
ALMA antenna emulator

Brent Carlson



ALMA antenna emulator

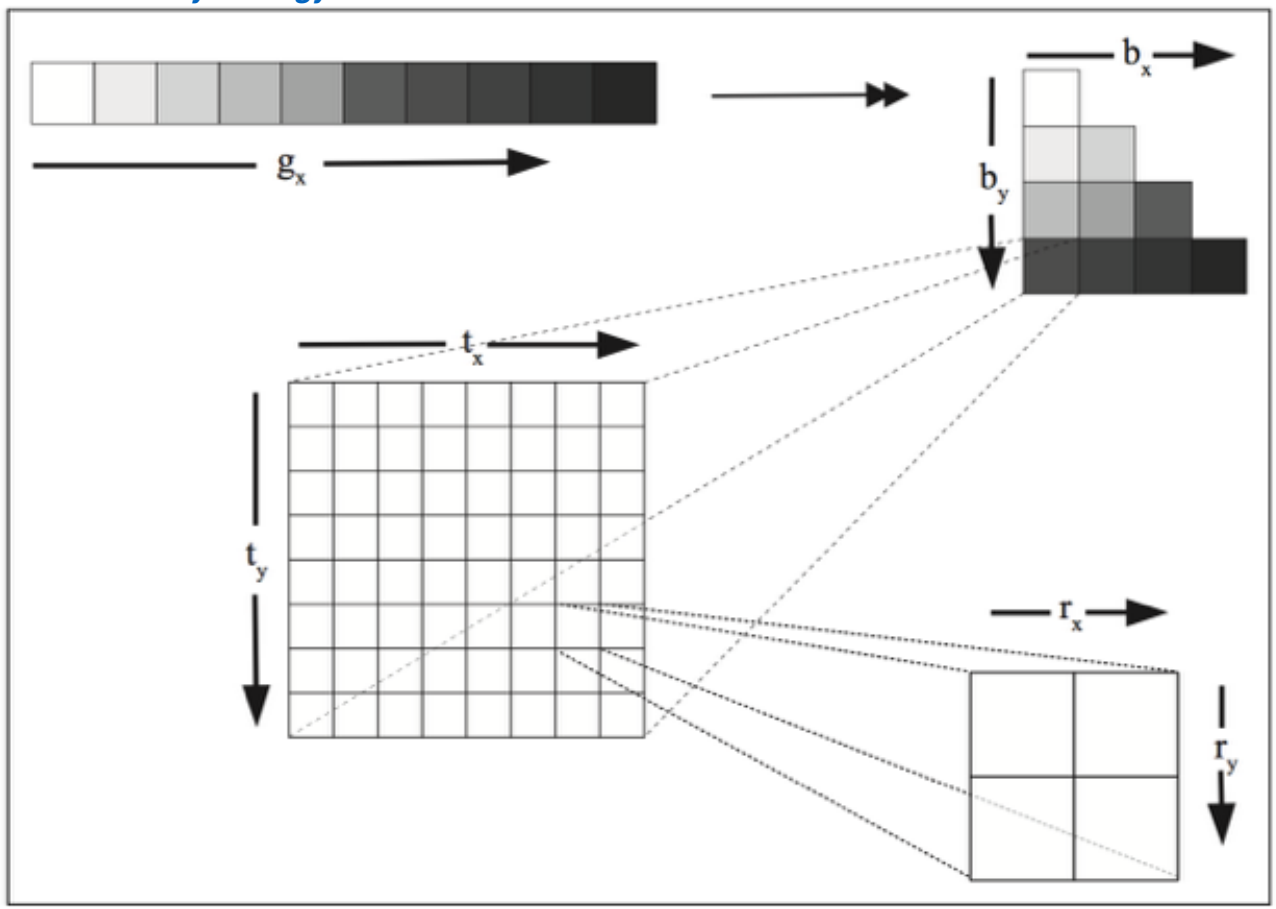
Brent Carlson



GPU X-engine

xGPU [Clark et al, 2012]

tiled memory strategy



triangular correlation matrix

sub-matrix calculated by single thread

Figure 3:. Schematic description of the how threads are mapped to the correlation matrix. The linear grid index g_x is mapped to the triangular block index (b_x, b_y). Each thread (t_x, t_y) within the thread block is then responsible for calculating an $R_x \times R_y$ tile of the correlation matrix (indexed by (r_x, r_y)). The grid index g_y maps trivially to the frequency dimension (not shown).

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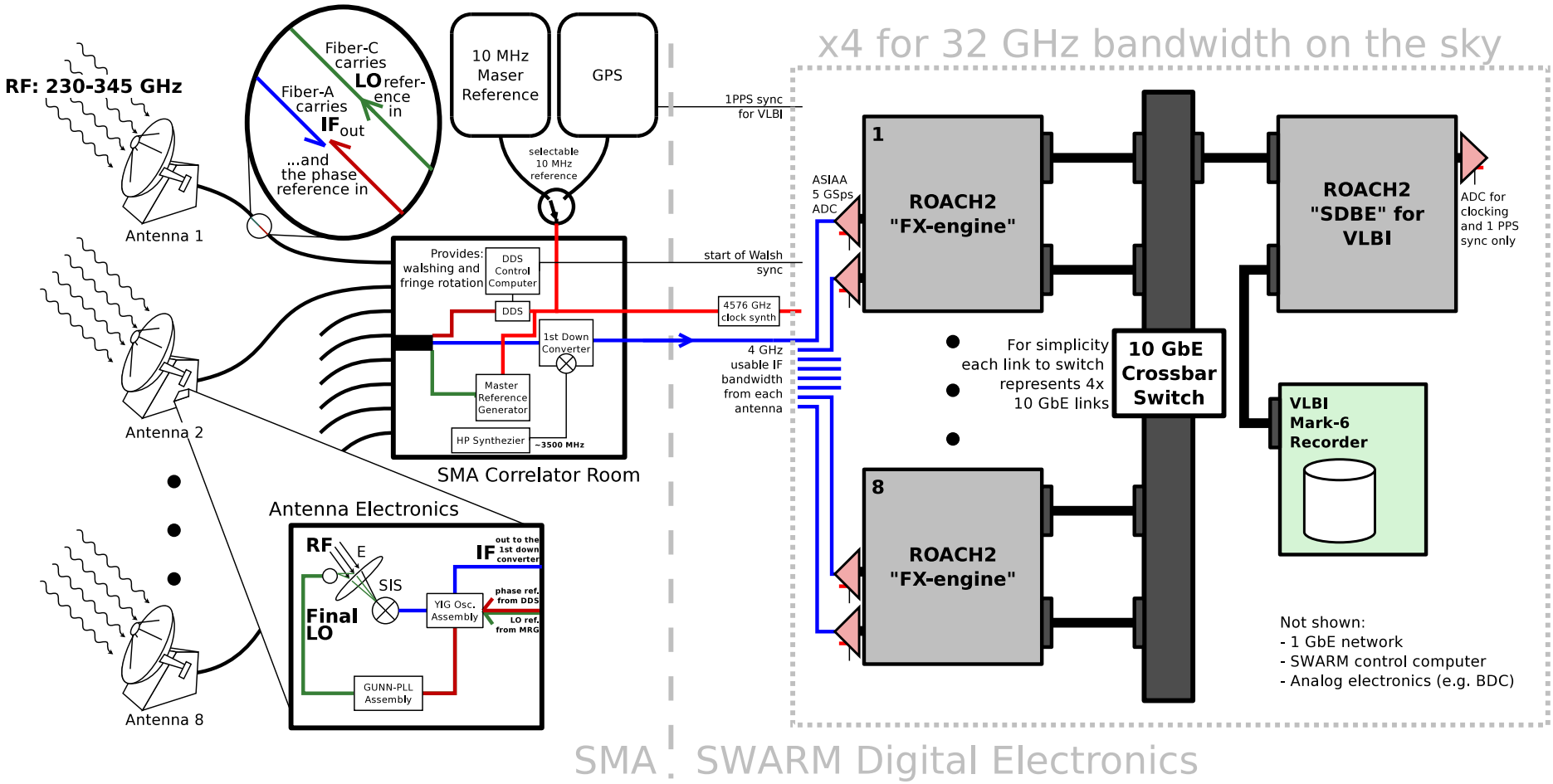
ASNT7122-KMA

15*GS/s*, 4-bit Flash Analog-to-Digital Converter with HS Outputs

- 20*GHz* analog input bandwidth
- Selectable clocking mode: external high-speed clock or internal PLL with external reference clock
- Broadband operation in external clocking mode: DC-15*GS/s*
- On-chip PLL with a central frequency of 10*GHz*
- Selectable on-chip PRBS 2^{15}-1 generator for output data scrambling
- Differential CML input clock buffer and output data and clock buffers
- Differential linear data input buffer
- LVDS input reference clock buffer
- Selectable on-chip digital-to-analog converter for self-testing

SWARM: SMA Wideband Astronomical ROACH2 Machine

(Primiani et al., JAI, 2016)



1 "quadrant": 2 GHz per receiver per sideband = 8 GHz; 32 GHz total

Benefits relative to ASIC correlator:

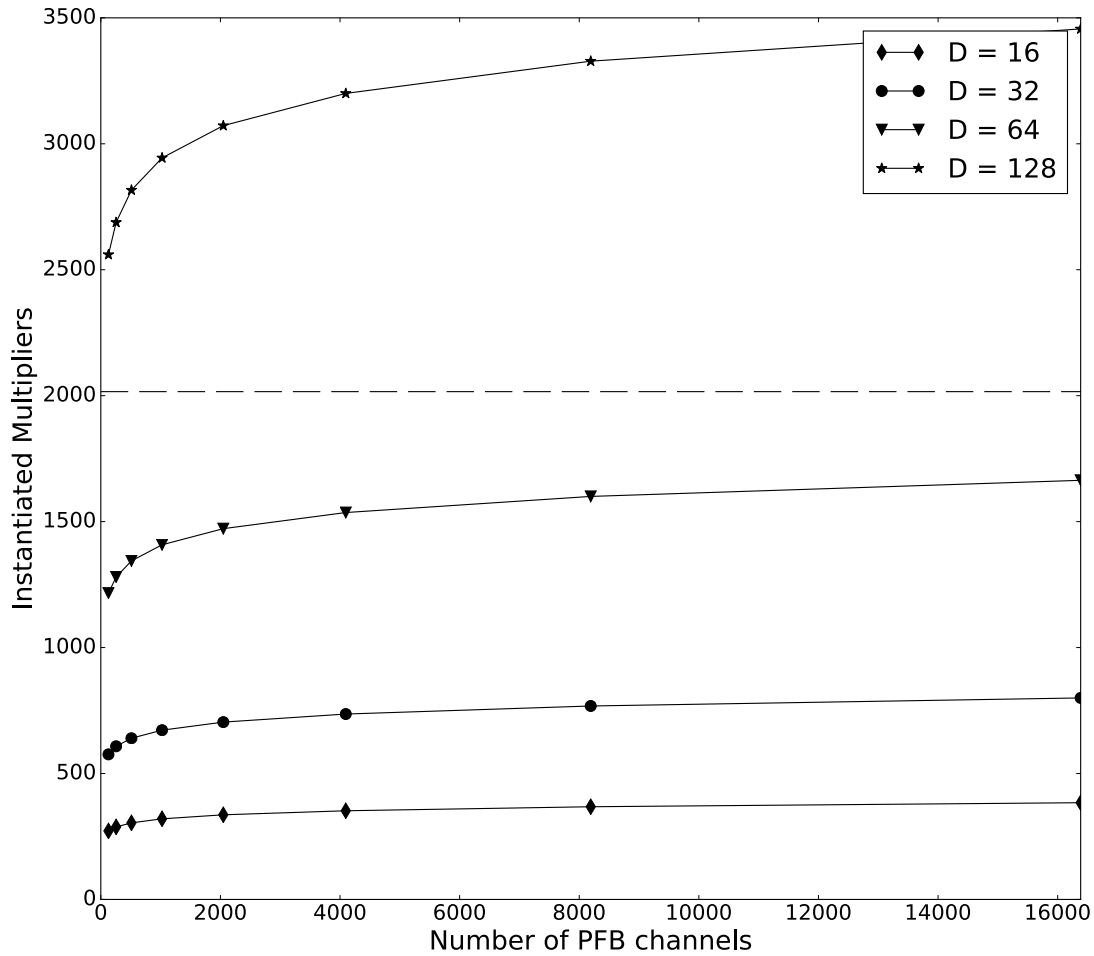
1. high uniform spectral resolution with no sacrifice of bandwidth,
2. smaller footprint and power consumption.
3. better digital efficiency with 4-bit cross-correlation
4. 2 GHz wide bands easier to reduce, result in higher quality spectra
5. Natively supports VLBI phasing and recording, 16 Gbps/quadrant
6. Built with CASPER and COTS components

“FPGA Utilization”: fine spectral resolution requires large FFTs

will all the SWARM logic fit?

(Primiani, Weintroub, deWerd, 2011,

https://www.cfa.harvard.edu/twpub/SMAwideband/MemoSeries/sma_wideband_utilization_1.pdf **)**

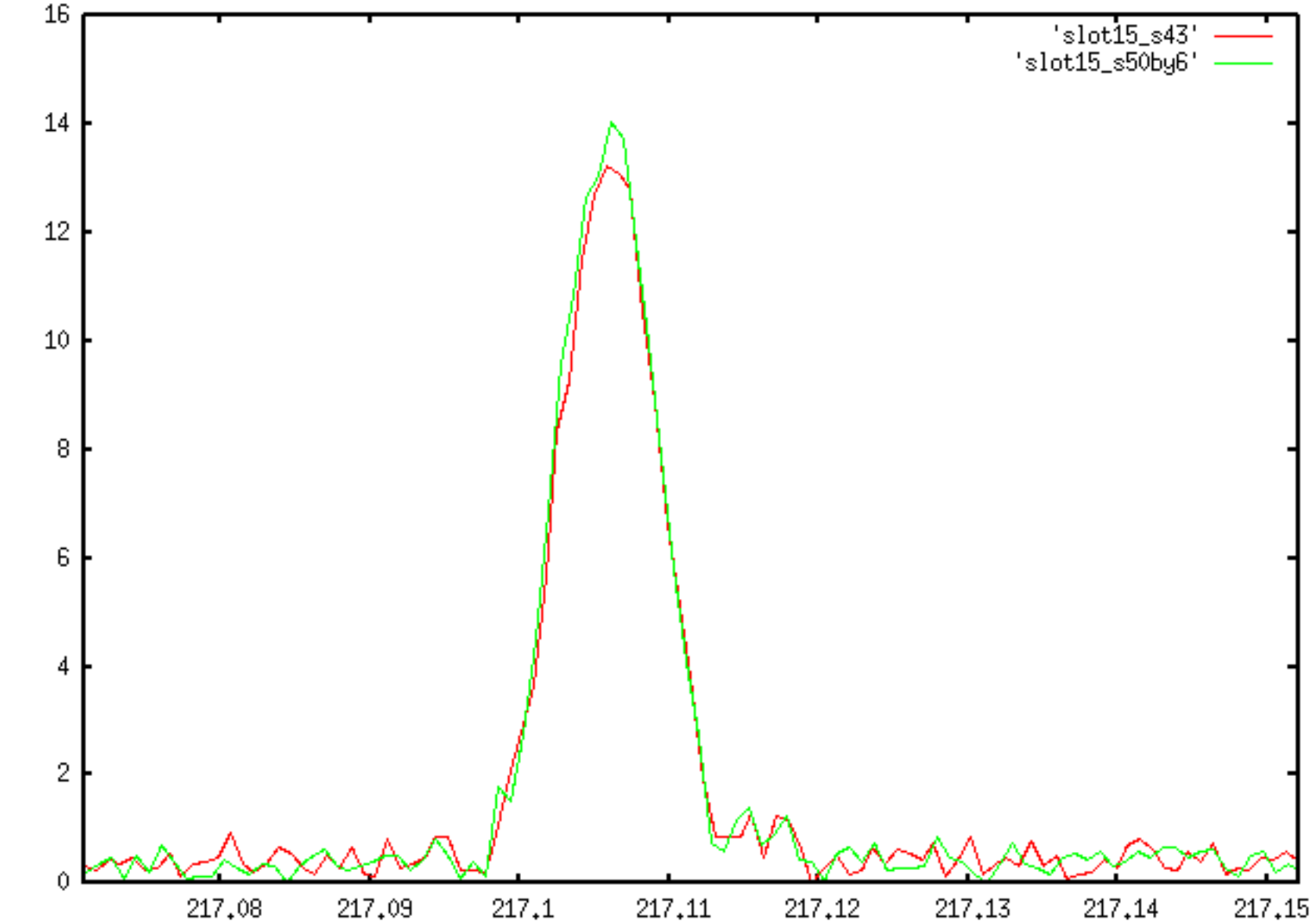


$$M_{\mathrm{PFB}} = \underbrace{D \log_2 ND}_{\mathrm{FFT}} + \underbrace{TD}_{\mathrm{FIR}} - \underbrace{2D}_{\mathrm{optimization}}$$

Example calculation of “instantiated multipliers” needed in FPGA for large “polyphase filterbank” (a type of FFT with improved isolation)

A 4-bit correlator is more efficient than 2-bit

SiO maser in R-Cas was used to measure the ratio of SWARM/ASIC SNR.



217.139, 6.48203 ASIC SiO line is red. SWARM line is green.

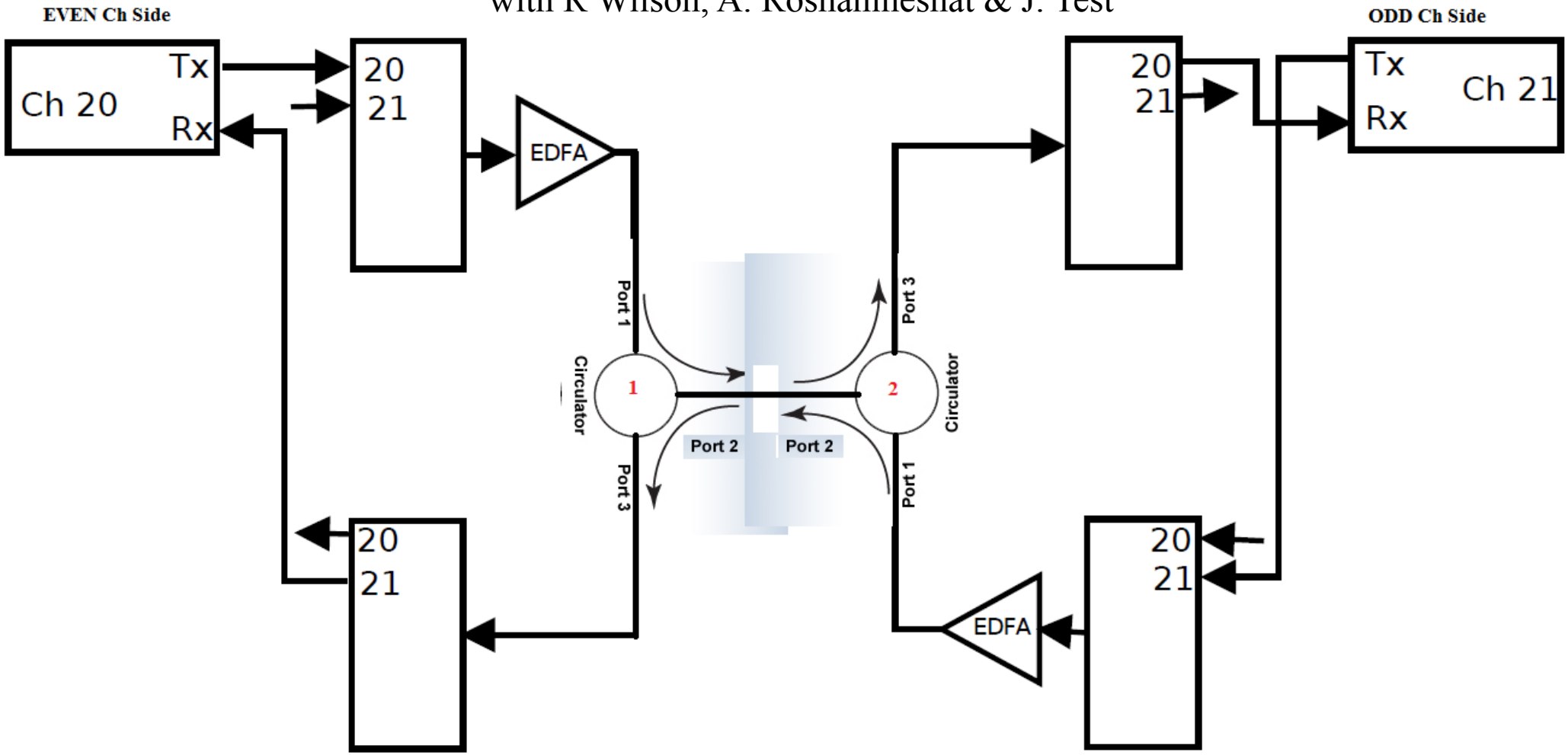
By measurement, SWARM SNR is 11 +/- 3% better

Yields about 70 extra days in a year of SMA operations

100 Gbps full duplex DWDM Ethernet on single fiber

(128 GHz bandwidth wSMA would require 8 100Gbps DWDM links per antenna)

with R Wilson, A. Roshanineshat & J. Test



DWDM: Dense Wavelength Division Multiplexing

Color-Z DWDM modules from Inphi