Submillimeter Array Technical Memorandum

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Date: April 9, 1993
From: Andrew Dowd

Proposed Downconverter Design

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I. Introduction

This document is a first attempt to solidify the design of the downconverter which is under development for the SMA. The discussion will not cover available converter options. Instead, I will focus on the design that is favored at this time. A brief overview of options was provided in SMA technical memo #63. The proposed design was covered in that memo along with some of its advantages and disadvantages. In this paper I will begin to focus on the implementation of the preferred architecture and examine some of the necessary parts. After outlining the design and discussing its ramifications, an estimate of system cost is given.

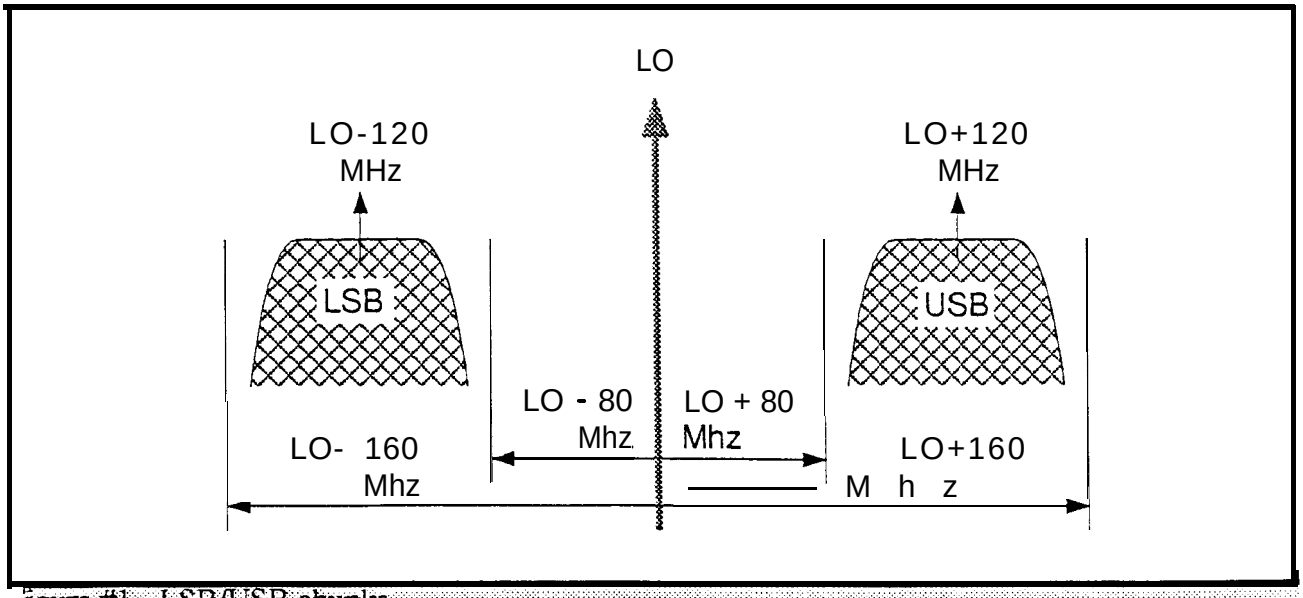
II. Downconverter Design

The architecture proposed for the SMA is a combination of the "frequency agile approach" and "frequency agile, both sidebands approach" described in sections II.C and II.D of SMA memo #63. Every "chunk" will be agile within the available IF band (The IF at this stage of the data chain extends from 4 to 6.040 GHz.) Most of the chunks will be somewhat encumbered by an opposing sideband which will move in lock step with the chunk (in frequency space). This limitation is necessary to reduce the cost of the image rejecting mixers, which are very expensive. This constraint is somewhat offset by the addition of some "free-agents". These chunks are essentially identical to the other mixers, except only one sideband is used (the other is terminated). Thus, these bands can be moved without the limitations imposed by the other sideband.

The first step in this converter review is a description of how the IF is subdivided into chunks. Next, I will discuss the hardware that goes into the downconverter. To this end, I will group the hardware into six subsections: the mixer, filter, sampler, station unit, computer and clock generator. The first four subsections are directly involved with data processing, while the last two are support circuits. This division of tasks is related to the physical divisions in the hardware.

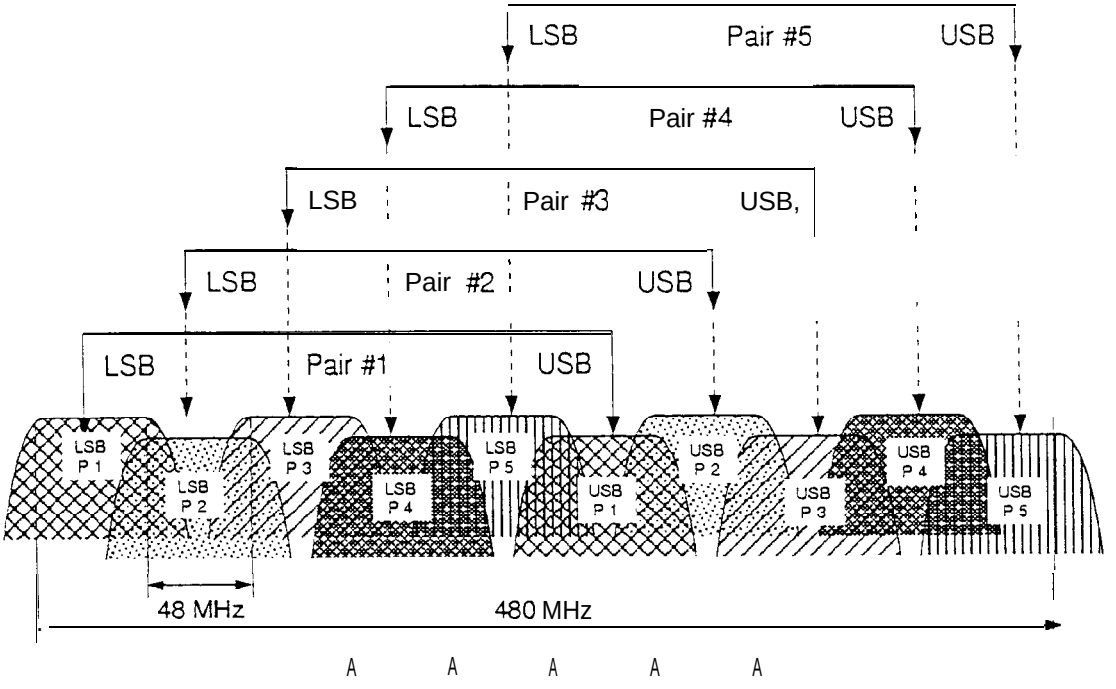
IIA. IF subdivision into "chunks"

The proposed design will use 34 chunks to cover the 2 GHz IF band. This is a slight increase over the original design which had 32 chunks per IF. The additional chunks can be processed by the correlator without any modification to its proposed architecture. The correlator design has always contained some extra correlators (they are required for 8 antenna mode), which will now be used to handle the two extra chunks in each IF band. The 34 chunks in each IF are composed of 1.5 "dual sideband" downconverters (which extract both the upper and lower sidebands independently to give 2 chunks per converter) and 4 single downconverters (which extract only one sideband). Both of the described converters are single-sideband, that is they reject the other sideband. The image rejection of the mixers will be specified as 30 dB(min), 40 dB (typ). The upper and lower sidebands from a dual converter are sketched in frequency space by figure #1.



igure #1 - LSB/USB chunks

Maximum Overlap Chunk Placement
BW = 1632 Mhz



	A	A	A	A	A
Block #1 LO's =	4,240	4,288	4,336	4,384	4,432
Block #2 LO's =	4,720	4,768	4,816	4,864	4,912
Block #3 LO's =	5,200	5,248	5,296	5,344	5,392

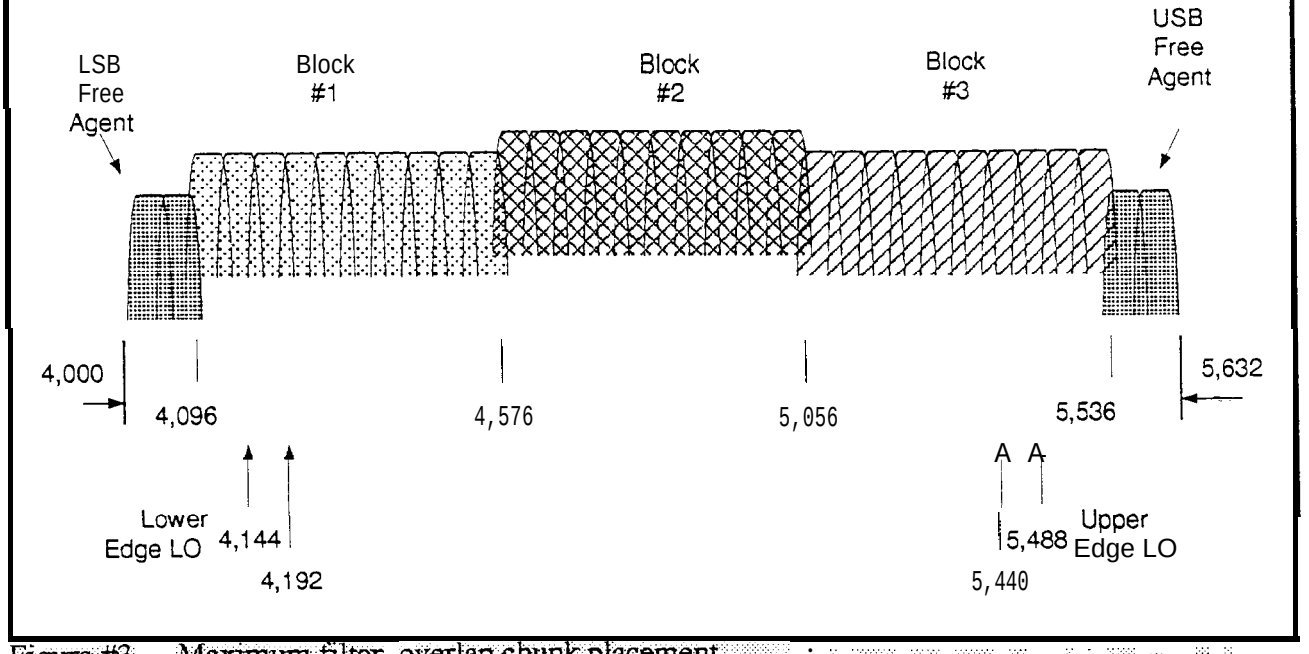


Figure #3 - Maximum filter overlap chunk placement

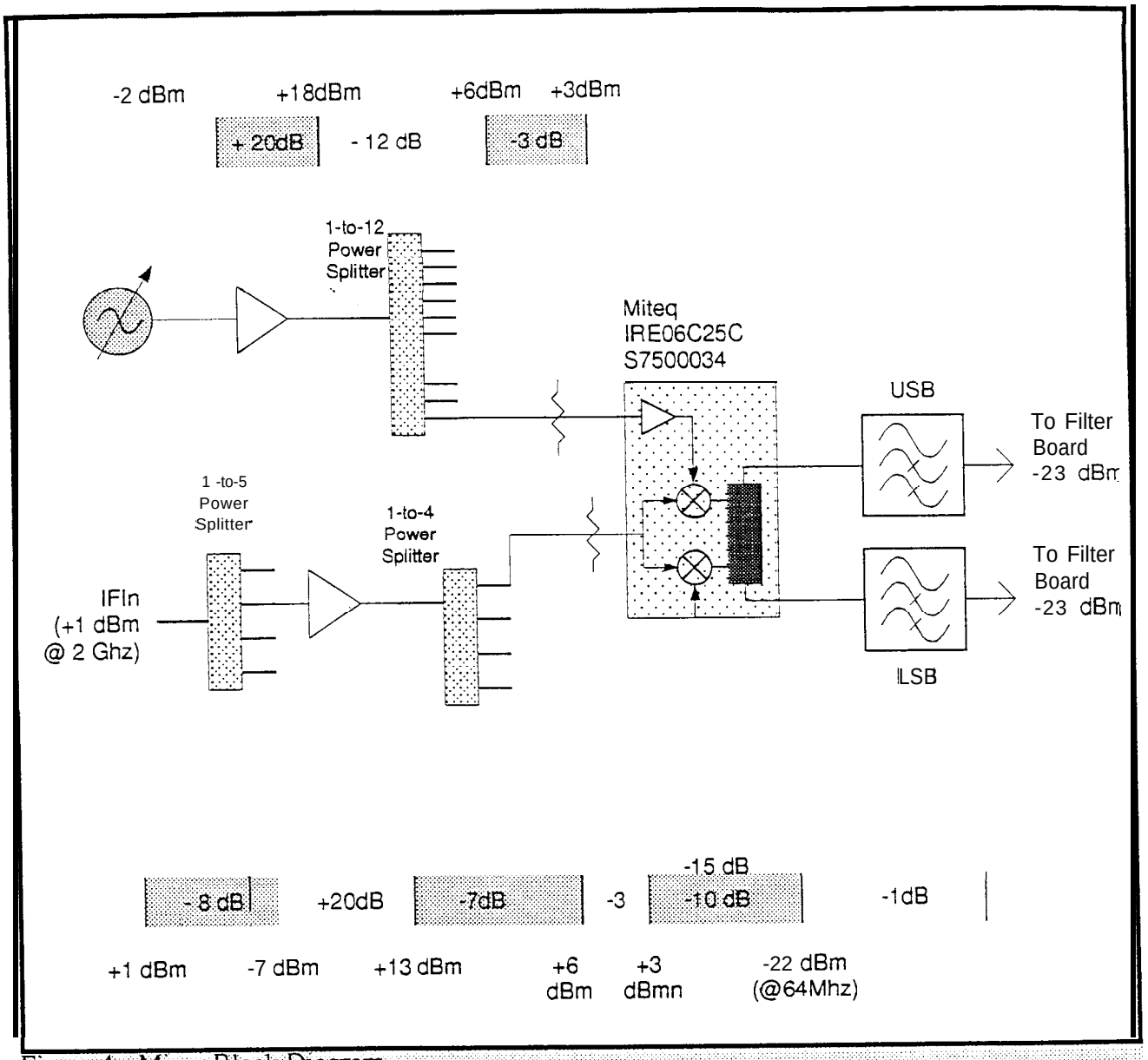


Figure 4 - Mixer Block Diagram

II.B. Mixer **Design**

The implementation of the chunk scheme outlined in the previous section requires two important components. First, a computer controlled LO with a minimum step size of 4 MHz (1 MHz preferred) and a frequency range of 4-6 GHz Second, an image rejecting mixer which produces both sidebands (USB and LSB), has image rejection of > 30dB, and an input RF band of 4 GHz to 6.04 GHz The availability of these two components creates an extremely simple downconversion scheme. This simplicity has great benefits in terms of maintance and also simplifies any leakage problem. Leakage is still a concern, but by performing the conversion in a single step, the "places" (in frequency and space) that are susceptible to leakage are reduced.

Figure 4 gives a block diagram of the proposed mixer design. The filter shown in the design is a mild, inexpensive one. Its main job is to reject high frequency leakage from entering the filter

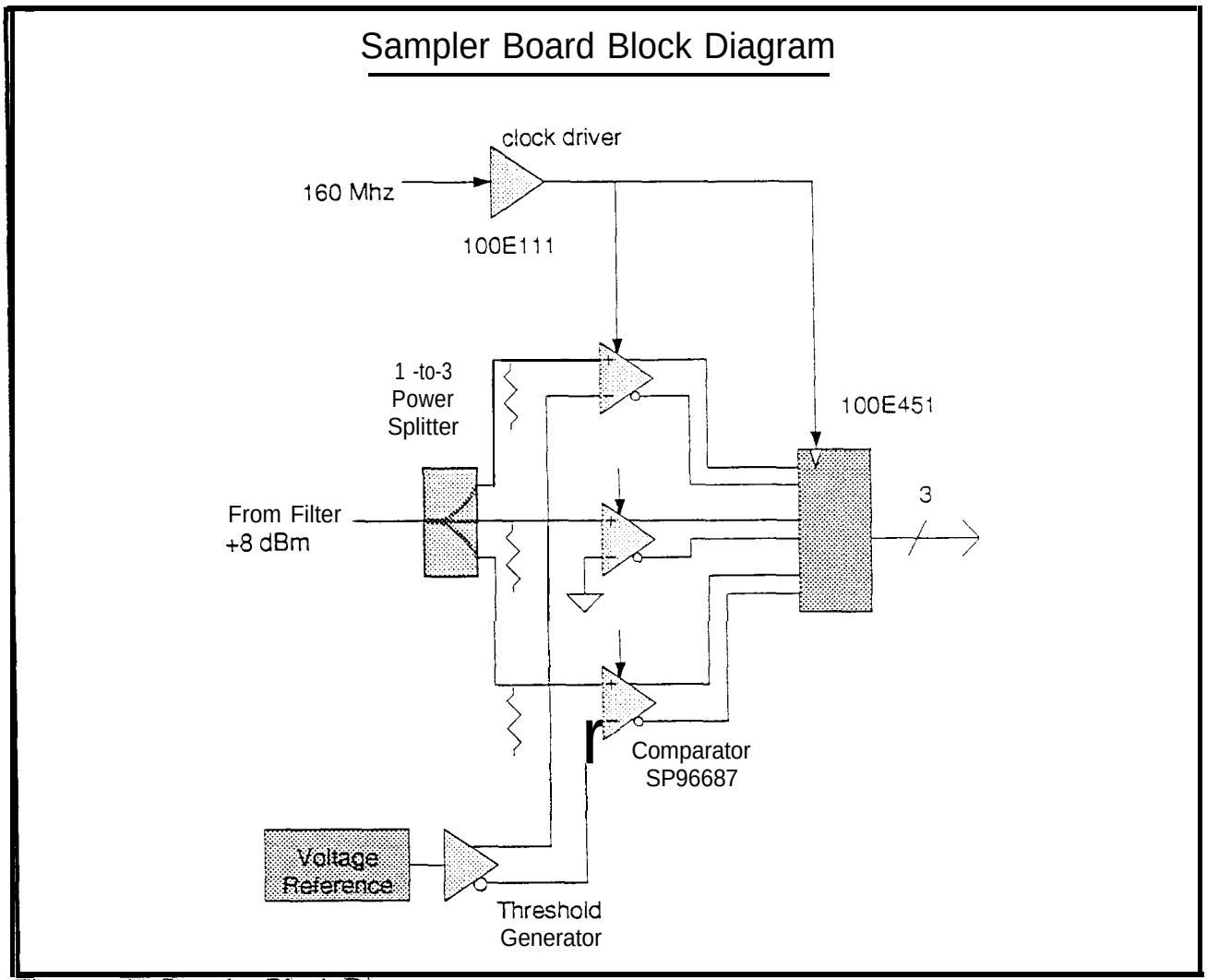


Figure 6 - Sampler Block Diagram

on a relatively inexpensive PC board. This will help minimize connector cost. The coupler which' links the power detector will be implemented as a resistive/stripline component. The electronic attenuator is used to fine-tune the power levels for optimum quantization. The primary level control will remain in the IF band with this unit used to correct mismatch between chunks and drift. The square law detector is necessary to measure the power within the band and "connect the chunks" into a flat baseline.

II.D. **Sampler design**

The next element in the signal process is the conversion to digital samples. A block diagram of the proposed architecture is presented in figure 6. Two important criteria for the sampler are isolation from digital noise and adequate dynamic range. To help isolation, the sampler PC board will be constructed entirely of surface mount components, with digital components on one side and analog on the other. An internal ground plane will help isolate the analog and digital signals. To improve dynamic range, a "true" power splitter will be used to help isolate the effects of impedance mismatch on the inputs to the comparators. Also, the comparator will have a much higher

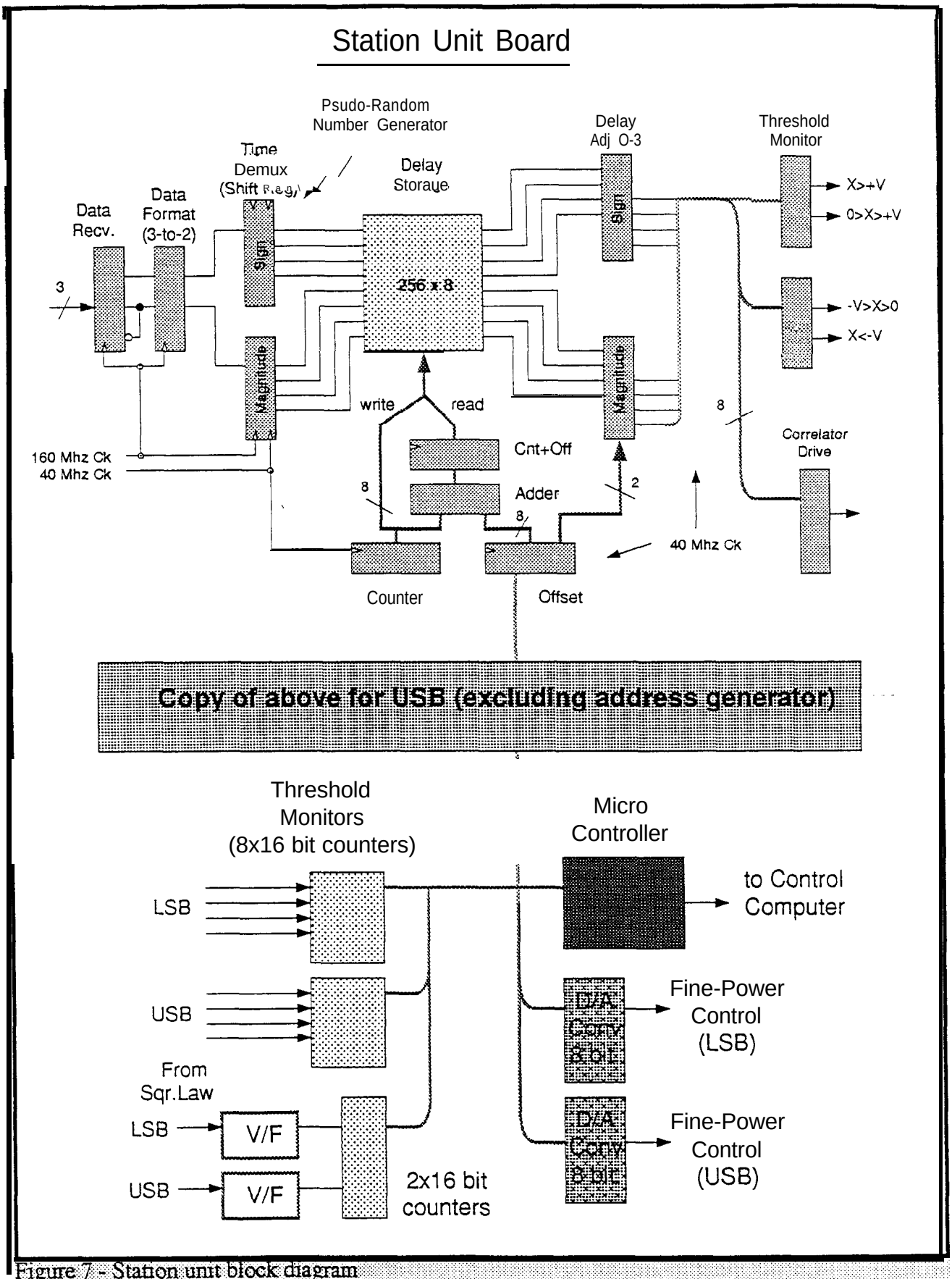


Figure 7 - Station unit block diagram

2.160 **MHz sampler clock -** This signal must also be locked to the system clock.

4.40 **MHz clock -** This will be derived from the 160 MHz clock. It must be centrally generated to ensure one sample accuracy of the delay system.

5.10 **msec cycle clock -** The fastest cycle of the phase switching (also Walsh switching), it has been recommended that this be generated here.

6. 320 **msec cycle dock** (may be distributed by software)

The LO reference and 160 MHz clocks will be somehow locked to the master telescoping timing clock. The 40 MHz clock will be generated from the 160 MHz. The 40 MHz clock will be sent to the correlator to resolve any timing skew during the station-to-baseline conversion. The slower clocks are important to many elements in the telescope (phase switching, correlator, etc.), and must be generated at one place, then distributed.

III. Downconverter costs estimates

Table 3 - Cost Estimates

III.A. **Non-recurring design charges**

Description	Total cost ($)
1. Sampler/filter board engineering charge	5000
2. Station unit board engineering charge	5000
3. Specialized design software	2000
4. Specialized test equipment	10000
	22,000

III. B. **Recurring costs (per unit charges)**

Description	Required quantity	Including spares	Estimated unit cost ($)	Total cost($)
1. Mixer - LO amp	236	244	**1825**	445,300
2. LO	19	21	3000	63,000
3. LO distribution	19	21	600	12,600
4. IF distr./amplifier	12	14	1000	14,000
5. Filter/sampler board	**408**	416	600	249,600
6. Station unit board	**204**	212	500	106,000
7. Connectors	**204**	212	100	21,200
8. Mechanical	**204**	212	200	42,400
				954,100

Net cost estimate of parts excluding labor and general test equipment: **$ 976,100**