The Receiver, Mezzanine and Backplane boards of the SMA Correlator

I. Introduction
II. Receiver Board
   II.A. Overview
   II.B. Description of Ports
      II.B.1. Sampler Input Port
         II.B.1.a. Sampler Data
         II.B.1.b. CLK Signal
         II.B.1.c. SYNC Signal
         II.B.1.d. RS-485 Asynchronous comm. port
         II.B.1.e. Receiver Recommendations
      II.B.2. Expansion Ports
      II.B.3. Hi-Res Ports
   II.C. Delay correction circuitry
      II.C.1. Data alignment circuitry
      II.C.2 Geometric Delay Compensation
   II.D. Sampler Statistics
III. Mezzanine Board
   III.A. Receiver Board Interface
   III.B. Clock
   III.C. BOCF generation circuit
   III.D. Walsh Clock input (320msec clock)
   III.E. Error Conditions
   III.F. VME interface
IV. Backplane
   IV.A Mezzanine Interface
   IV.B. Correlator Board Interface
V. Test Procedures
Appendix A Pin out of Sampler connector
Appendix B Pin out of Expansion Port
Appendix C Pin out of Hi-Res Port
I. Introduction

This document is an functional description of the correlator subsystem that accepts data from the samplers and drives the input connector of the correlator boards (See MIT Haystack Obs. "Correlator Board Hardware Specification"). This subsystem consists of three electronic modules which reside within the correlator crate. These modules are PC boards which will be called: the Receiver board, the Mezzanine Board and the Backplane. The intent of this document is to produce a comprehensive description of this system as viewed by a potential user. There is no attempt to define the interface between these boards or to the correlator board. This document will describe the operational capabilities of the design and interface specifications that pertain to the hardware interface (i.e. sampler input). Also, there is a detailed description of two lateral connections that implement some additional correlator modes.

II. Receiver Board

II.A. Receiver Board - Overview

The receiver board accepts signals directly from the sampler and performs several signal processing steps before sending the sampled data stream to the mezzanine board. The processing necessary includes, alignment of data streams, geometric delay compensation and state counting. These functions will be elaborated in detail their respective descriptions. The receiver board also provides resources to implement some correlator modes which require the same sampler data to reach more than a single correlator chassis. For most modes, data from a given sampler is drive across a single chassis. However, for two special cases, it is necessary to re-transmit a copy of the sampler data to another chassis. The receiver board provided extra input/output resources to support these special cases, plus the necessary multiplexing to support these modes.

II.B. Description of the Ports

The receiver board has 2 direct sampler inputs (from the analog portion of the correlator) and 2 expansion ports, which are shadows of the sampler inputs. Also, the receive board has 4 "Hi-Res" input ports which are used to implement correlation modes that extend beyond a single chassis. To drive the Hi-Res ports, there are 6 Hi-Res output ports. The mismatch in Hi-Res in/out ports will mean some outputs in some chassis will be unused.

II.B.1. Sampler Input Port

This input connection introduces data from the sampler into the correlator system. The 2-bit sampler data is demultiplexed by a factor of 4 to create one byte of data per 52 MHz clock. To consolidate cabling, each connector will contain the data from 4 samplers. This means 32 sampler signals per cable. To minimize transfer errors, the data will be sent full differential. This increases the number of signals to 64.

This connector also contains 4 additional signals, all of which are differential. The other signals include the 52 MHz data clock, a data SYNC, and an RS-485 communications port which is full duplex so there is a transmit and receive signal. The functional details of these signals are described in the following sections.
The drive and cable will be matched for a 50 ohm termination.

**Connector Type** ................................................................. Part #N10280-5242VC

**Pin Count** ................................................................. 80

**Cable Type** ................................................................. (TBD)

See appendix A for a pin-out of this connector.

### II.B.1.a. Sampler Data

The samplers operate at 208 Msamples per second. After demultiplexing, the data rate on the sampler cable becomes 52 Mbits per second.

Sampler data consists of demultiplexed 2 bit data samples. Data encoding is in the form of Sign/Magnitude as described in “CMOS Correlator Preliminary Product Specification by John Canaris, p.12. There is no validity bits encoded with the sampler data. The data is fully differential. It will be encoded such that Logic “High” is represented by an ECL “High” (v > -1 volt) on the non-inverting line, from this it follows that the inverting line will have an ECL “Low” (v < -2 volts). All future references to logic levels (high, low, rising, falling) will be a reference to the non-inverting signal, with the inverting signal always acting in a complementary fashion.

**Bit Rate** ........................................................................ 52 MSamples per sec.

**Setup Time to Data Clock** ................................................... TBD(min)

**Hold Time to Data Clock** ................................................... TBD(min)

**Signal Level** ................................................................ Differential 100K ECL

**Impedance** ................................................................ 50 ohms

**Data Bit to Data Bit Skew** .................................................. TBD(max)

### II.B.1.b. CLK Signal

This clock will be used to capture the incoming data. Each sampler cable has its own clock. There are 72 independent clocks will have different phase relationships. All CLKS are derived from an single source, but may travel over different paths. However, the clock will be registered with the data. Thus, the clock which arrives on the sampler cable can be used to capture the data on that cable.

**Frequency** ........................................................................ 52 MHz

**High Period** ......................................................................... 7 nsec (min)

**Low Period** ........................................................................ 7 nsec (min)

**Signal Level** ................................................................ Differential 100K ECL

**Impedance** ................................................................ 50 ohms

### II.B.1.c. SYNC Signal

Each sampler cable will contain a SYNC signal. This signal provides a reference for aligning the incoming data samples. The data generator must apply a relative delay in the various data streams. The reference point for the digital delay will be the rising edge of this sync signal. (See Section ??). To fulfill this role, it must reliably mark a single clock cycle. Therefore, it must be clean captured by the clock. It is derived from a common source, so maintains a fixed relative phase relationship.
However, the copies that arrive at the various sampler input ports will travel over various paths, so it will be necessary perform some realignment on the data streams to ensure consistent systematic delay.

The falling edge of the SYNC should be used for error checking only.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Frequency</td>
<td>100 Hz(10msec)</td>
</tr>
<tr>
<td>Active Period (Logic High)</td>
<td>5 µsec &lt; T &lt; 100 µsec</td>
</tr>
<tr>
<td>Hold Time (to CLK)</td>
<td>TBD</td>
</tr>
<tr>
<td>Setup Time (to CLK)</td>
<td>TBD</td>
</tr>
<tr>
<td>Signal Level</td>
<td>Differential 100K ECL</td>
</tr>
<tr>
<td>Skew: Sampler-to-Sampler Input</td>
<td>± 10 clock cycles</td>
</tr>
<tr>
<td>Skew: Sampler/Expansion/H-Res port</td>
<td>(TBD)</td>
</tr>
</tbody>
</table>

II.B.1.d. RS-485 Asynchronous comm. port

The sampler board houses a microprocessor which will be used for control of analog signal processing chores. Two-way communications from this micro and crate controller is performed over an asynchronous communications port. To avoid receiver error the data is transmitted differentially using RS-485 type drivers. (Note the drive characteristics are the only aspect of RS-485 which are observed).

a small phase rate correction will be performed in the last LO. There will be a microprocessor which controls the phase rate for four (4) chunks. Conveniently, the same four chunks that exist on the 80-Pin cable from the Sampler Driver will be control by a single micro. Therefore, to simplify wiring, the communication to this micro will be placed on the sampler cable. (The micro is physically close to the sampler board). The format of this communication will be Asynchronous full duplex differential TTL. It should use RS-485 type drivers/receivers (See 75ALS181). The correlator side of this communication port should be accessible from the VME bus. This link carries information about RF power level in an analog Chunk, plus status information.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Baud Rate</td>
<td>406.25 Kbits</td>
</tr>
<tr>
<td>Input Hardware buffer size</td>
<td>64</td>
</tr>
<tr>
<td>Signal Level</td>
<td>Differential TTL, RS-485</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 ohms</td>
</tr>
</tbody>
</table>

II.B.1.e. Receiver Recommendations

The Samplers and Receiver boards will resided in different rooms over a moderately long cable. To minimize potential reception problems, the receivers will be differential with some common mode rejection. Also, the only ground return path, will be small (the cable shield ??). Therefore, the input current leakage should be minimized to avoid ground loop problems. The receiver should be chosen to have maximum common-mode range and minimum input leakage current.

II.B.2 Expansion Ports

These connectors simulate a sampler output. These connections will provide support for the correlator expansion to handle 8 SMA antennas. The proposed expansion will double the correlator...
performed on the backplane

Total Power Dissipation.............................................................................................................. (TBD)
Voltage........................................................................................................................................ (TBD)
Current ........................................................................................................................................ (TBD)

(...more..)

V. Test Procedures

V.A. Sampler Loop Back Test for Receiver Board
Connect a source to the sampler input. Connect a “loop” back cable from the Expansion port of the active sampler input to the other sampler input. (more)

V.B. Hi-Res Port loop back test.
(... more...)

V.C. Asynchronous Comm Port Loop Back Test
(... more...)

Appendix A - Pin out of Sampler cable

1. GND
2. ~SAMP_1_MS_D0
3. ~SAMP_1_MS_D1
4. ~SAMP_1_MS_D2
5. ~SAMP_1_MS_D3
6. ~SAMP_1_LS_D0
7. ~SAMP_1_LS_D1
8. ~SAMP_1_LS_D2
9. ~SAMP_1_LS_D3
10. ~SAMP_2_MS_D0
11. ~SAMP_2_MS_D1
12. ~SAMP_2_MS_D2
13. ~SAMP_2_MS_D3
14. ~SAMP_2_LS_D0
15. ~SAMP_2_LS_D1
16. ~SAMP_2_LS_D2
17. ~SAMP_2_LS_D3
18. ~SAMP_3_MS_D0
19. ~SAMP_3_MS_D1
20. ~SAMP_3_MS_D2
21. ~SAMP_3_MS_D3
22. ~SAMP_3_LS_D0
23. ~SAMP_3_LS_D1
24. ~SAMP_3_LS_D2

41. GND
42. SAMP_1_MS_D0
43. SAMP_1_MS_D1
44. SAMP_1_MS_D2
45. SAMP_1_MS_D3
46. SAMP_1_LS_D0
47. SAMP_1_LS_D1
48. SAMP_1_LS_D2
49. SAMP_1_LS_D3
50. SAMP_2_MS_D0
51. SAMP_2_MS_D1
52. SAMP_2_MS_D2
53. SAMP_2_MS_D3
54. SAMP_2_LS_D0
55. SAMP_2_LS_D1
56. SAMP_2_LS_D2
57. SAMP_2_LS_D3
58. SAMP_3_MS_D0
59. SAMP_3_MS_D1
60. SAMP_3_MS_D2
61. SAMP_3_MS_D3
62. SAMP_3_LS_D0
63. SAMP_3_LS_D1
64. SAMP_3_LS_D2
to 12 chassis from the original 6 to handle the 8 antenna SMA, which has 28 baselines instead of 15. Since the expansion will be done after the commissioning of the 6 antenna system, we’ve proposed an expansion which would have a minimal impact on the existing hardware.

This expansion port is a buffered and re-clocked image of a sampler cable. Thus, an expansion port could be used to drive a sampler input on another receiver board. In general, the pinout of the “expansion” connector should be identical to the sampler connector (albeit an output instead of an input). There is one exception that makes the “expansion” cable different from a “sampler” cable. Because there is no analog control micro at the end of an “expansion” cable, there is no terminus for the RS-485 communications port. Thus, one solution would be to disregard the RS-485 signal for the “expansion” cable. However, there is a case to be made for allowing the information which is sent back from the sampler to be copied and re-transmitted down the expansion cable. This would allow the expanded chassis to read the total power information which is returned by the samplers. Otherwise, this information would need to be distributed through the computer network, which would create unnecessary overhead.


To perform high resolution processing of correlator data, it will be necessary to distribute sampled data from one chassis to others. In most correlators this distribution is performed AFTER the data has passed thru the correlator delay chain. However in this case we can avoid the need by separating the various sub-correlations which are performed after demultiplexing the data. The cables that I propose using are Point-to-Point Cable Assemblies for example: Amp Part #620389-1. For the PC board connector this requires a Square or Round posts 0.025” in an array of 0.1” spacing.

The Hi-Res outputs will have buffered and re-clocked sampler data, plus a copy of the (sampler generated) clock and SYNC signal. Thus, the signals will be ready for re-synchronization by the receiving chassis. The Hi-Res Inputs will allow accept the Hi-Res signals from another chassis and switch them into the sampler’s data path (See below). Because this path will contain its own sync signal, the problem of data cable delays from the Hi-Res cables can be handled using the proposed FIFO hardware.

The data portion of the Hi-Res ports will be the 8 bits of information that make up the demultiplexed data stream (2 bits per sample, 4 samples per 52 MHz clock cycle). These will be send differentially and include a ground connection. Thus, each signal will have 3 pins. The data signals will appear as a 0.1 grid which is 3x8 in size. To carry the Sync and Clock, there must be to additional differential signal paths. Thus, each Hi-Res port should will be a grid of 3x10.

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**Connector Data**

<table>
<thead>
<tr>
<th>Connector</th>
<th>N 10280.5242VC</th>
</tr>
</thead>
<tbody>
<tr>
<td>Active Period (Logic High)</td>
<td>10usec &lt; T &lt; 100usec</td>
</tr>
<tr>
<td>Signal Level Data, Clock, Sync</td>
<td>Differential 100K ECL</td>
</tr>
<tr>
<td>Signal Level Comm port</td>
<td>Differential TTL, RS-485</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 ohms</td>
</tr>
<tr>
<td>Ports per Receiver Board</td>
<td>2</td>
</tr>
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</table>

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**Connector Data**

<table>
<thead>
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<th>Connector</th>
<th>TBD</th>
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</thead>
<tbody>
<tr>
<td>Active Period (Logic High)</td>
<td>10usec &lt; T &lt; 100usec</td>
</tr>
<tr>
<td>Signal Level Data, Clock, Sync</td>
<td>Differential 100K ECL</td>
</tr>
<tr>
<td>Impedance</td>
<td>50 ohms</td>
</tr>
</tbody>
</table>
II.C. Delay correction circuitry

II.C.1. Data alignment circuitry

Data samples will arrive from four possible sources: the two sampler cables and the two HI-Res ports. (There are 4 Hi-Res inputs on each receiver board, but only two are active simultaneously.) As a consequence there can be 4 “independent” SYNC signals operating on each receiver board.

The different SYNC signals represent four data streams which can have arbitrary delay/phase. (The various data streams can be skewed by up 10 clock periods). The receiver circuitry must be able to properly receive each of the data streams and align them, relative to their respective SYNC signals.

Each of the SYNC signals will operate an independent alignment circuit. However, one and only one of these SYNC signals must be selected for transmission to the mezzanine board as a candidate for the master SYNC. The selected sync which will go to the mezzanine board will be called SSYNC to avoid confusing it with the four received versions.

Sync Skews ......................................................................................................................... clock periods

II.C.2 Geometric Delay Compensation

To correct for travel time across the array, requires variable delays in the digital data stream. The maximum digital delay required by the SMA is related to the physical size of the array and any telescope cabling delay differences. We must also be sure to handle the (longer) baselines associated with the JCMT/CSO link up.

The data is processed by this board after it is demultiplexed. However, we need the ability to apply a delay resolution of one data sample. This means any delay (which is not a factor of 4) will need a fine delay correction that rolls the data between the bytes received every clock cycle.

The rate-of-change of the delay value is quite slow. Worst case, the delay will change by one sample period every minute when we are tracking a source. (The delay will jump when we move to an new source, but in this case there is lots of time before the telescope can slew to the new source) Therefore, it would be acceptable to restrict delay changes to fall during the sync period of a new cycle (320ms). Also, these delay changes should ALWAYS be applied during the blanking period which precedes the sync signal. Since delay changes are infrequent, the delay will be fully buffered the most recently loaded delay value will be used repeatedly. Thus, it will not be necessary for the computer to reload this value, unless it changes.

Digital Delay Range (without Sync Skew) ......................................................... 0 4096 Data Samples
Delay resolution.. ........................................................................................................ 1 Data Sample
Total Throughput delay.. ..................................................................................... TBD
Delay Modification frequency.. ......................................................................... Every 320 msec
II.D. Sampler Statistics
The SMA correlator will have fixed sampler thresholds voltages which may vary from optimum by a small amount. To correct the data for any effects due to sub-optimum threshold levels, requires an estimate of threshold voltages. The easiest method to get this value is to measure the relative occurrences of the states (e.g. 00) in the sampled data stream. Since it is possible to have asymmetric voltage levels, it is necessary to measure ALL the state occurrences. It would be possible to extrapolate one of these measurements using the measurement of three others and the integration time. However, for simplicity, all 4 occurrences should be measured (i.e 00,01,10,11). This measurement must be made on all 288 active samplers.

This measured value number will vary quite slowly. Thus, it would not be necessary to get this value back to the VME controller every 10msec. The hardware counters should transfer these values to secondary storage on the rising edge of the SSYNC or MSYNC, but only on the when the Walsh clock is asserted (See section II.D.). Unread values should be overwritten.

This data can be corrupted by switching transients in the data streams which occur during every sync period. Therefore, these counters will be blanked during the same period as the correlation data. (See Section II.C.).

Prescalar bits ................................................................. 4(max)
Counter Depth ................................................................. 28 bits (less prescalar)
Buffering ................................................................. Fully Double buffering
Transfer to buffer signal ................................................................. 320 msec tick
Data Statistics Measured ................................................................. {00,01,10,11}

III. Mezzanine Board

Rec boards supported ................................................................. (!)
Data Rate ................................................................. 52 MHz (min)
Total Power Dissipation ................................................................. (TBD)
Voltage ................................................................. (TBD)
Current ................................................................. (TBD)

III.A. Receiver Board Interface

III.B. Clock
Each receiver board will produce an independent SCLK (52 MHz). One version of this signal will be chosen (via MUX) as the “master” clock for all the correlator boards. To avoid confusion, the selected SCLK signal which that will be used by the mezzanine board will be called MCLK.

III.C. BOCF Generation
Every receiver board produces an independent SSYNC signals. A multiplexer will select one version of this signal must be chosen to act as the master timing synchronization signal for use in BOCF generation for the entire crate. To avoid confusion, the selected SSYNC signal which will be used by the mezzanine board will be called MSYNC. The source of the MSYNC signal should be
identical to the source of the MCLK, which should be enforced by using the same register value to drive both multiplexer controls.

The mezzanine board will have two counters to control generation of the BOCF signal required by the correlator boards. Both counters will operate at 52 MHz. The first counter will be started by the arrival the rising edge of MSYNC. It specifies the “dead period” in which incoming data is to be ignored. When this counter completes, the BOCF should be driven low and the second counter begins. The second counter will define the period in which data is processed by the correlator board. When this counter terminates, BOCF should be pulled high to end the correlation.

Dead period length............................................................... .24 bits(min)
Correlation period length.................................................. .24 bits(min)

III.D. Walsh Clock input (320msec clock)

This signal will be generated via computer and not hardware. Therefore, it can have a very wide phase variance (relative to the 10msec tick which is fixed). It will NOT be possible to cleanly capture this signal with the 52 MHz cm-relator clock. It will be guaranteed to be stable during the “SYNC” trigger. Thus, it will be stable for at least 1 microsecond before and after the “SYNC” trigger. It will have adequate margin provide the full 1 microsecond margin for ALL versions of the “SYNC” signal.

Hold Time (to SSYNC) ........................................................................ |   msec(min)
Setup Time (to SSYNC) ...................................................................... |   msec(min)

III.E. Error Conditions

There will be circuitry on the mezzanine board to detect and report errors to the crate controller. Some of the error conditions which should be detected include the loss of sync and loss of clock. Also, since the correlator control signals are general counter values, it would be possible to program with values that create conflicts. For example, if the falling edge of the BOCF occurs before the “ready-to-read” of the FIFO. Another case would be the falling edge of the BOCF occurring before the falling edge of the SSYNC. Another error condition would be created if counter #2 indicates the end of the cycle (rising edge of BOCF) after the arrival of the rising edge of SSYNC.

Another important error condition is data overflow in the Asynchronous communication ports.

III.F. VME interface

To allow computer control and communication with the crate controller, the mezzanine board must have a VME interface. This interface will allow A32/D32 addressing and consume no more than (TBD) megabytes of the A32 address space. Location of address space should be selectable using on-board dip switches.

Read/Write cycle time........................................................................... (TBD)
Address Space....................................................................................... (TBD)(Max)

IV. Backplane

The backplane serves as a passive interface from the mezzanine board to the correlator boards. Much of the the distribution of station (antenna) data streams to calculate the various baselines is
<table>
<thead>
<tr>
<th></th>
<th>Description</th>
<th></th>
<th>Description</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>25</td>
<td>~SAMP_3_LS_D3</td>
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<td>SAMP_3_LS_D3</td>
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<tr>
<td>26</td>
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<td>66</td>
<td>SAMP_4_MS_D0</td>
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<td>33</td>
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<td>-CLK</td>
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<tr>
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<td>GND</td>
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<tr>
<td>36</td>
<td>-SYNC</td>
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<td>GND</td>
<td></td>
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<td>38</td>
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<td>RX-DATA</td>
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<td>79</td>
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<td></td>
</tr>
<tr>
<td>40</td>
<td>-TX-DATA</td>
<td>80</td>
<td>TX-DATA</td>
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</table>

Appendix B Pin out of Hi-Res Cable
(TBD)