FIGURES-PART 1
Figure 1.1. The MIRAC cryostat. All dimensions shown are in inches.

1.1a. Cutaway view from the side, showing the internal mechanisms. A ray tracing of the optical beam is shown entering the dewar from the left. The array sliding stage is shown in the low magnification position; below it are the filter wheels and then the pupil stop slide, which moves perpendicular to the plane of the paper. The actuators are shown partially inserted-- during normal operation, these are withdrawn outside the LN$_2$ radiation shield to eliminate unnecessary heat load.
Figure 1.1b. MIRAC array mounting assembly. The array is mounted in a socket on top of the stage. A copper "finger" extends through the socket and makes direct contact with the backside of the chip carrier, through a piece of indium foil. The copper mount that holds the array and circuit board is insulated from the rest of the dewar by a G10 spacer, and the thermal connection is made using a flexible copper strap below the stage. Detents and spring-loaded balls define the two magnification positions.
Figure 1.1b
Figure 1.1c The MIRAC cryostat, top and bottom view.
Figure 1.1d. The MIRAC cryostat, cutaway section view from the bottom.
Figure 1.1e. MIRAC filter wheels, number 1 on the top and number 2 on the bottom.
Figure 1.2. MIRAC Optics ray diagram. The position of the dewar window and radiation shield baffles are indicated. The units are in cm. In changing from low to high magnification, the only change is in the position of the array and the focus position outside the dewar.
1.2a. Low magnification position.
Figure 1.2a.
Figure 1.2b. MIRAC optics High magnification position.
Figure 1.3. Hughes IBC detector cross section, from a figure provided by Hughes and published by Fowler and Joyce (1990). Two pixels are shown on the left, and the guard ring and electrode are shown on the right. The indium bumps allow for bonding to the readout array.
Figure 1.4. Hughes IBC 20x64 detector layout, from a figure provided by Hughes and published by Fowler and Joyce (1990). The array is organized as two 10x64 sub-arrays, separated by a pixel and offset by a half pixel in the long dimension, surrounded by a guard ring.
Figure 1.5. Hughes Si:As IBC detector spectral response, from data supplied by Hughes. This response was not measured for the particular device used in MIRAC, but represents the general response of this detector material. The "photon response" or quantum efficiency is plotted as a function of wavelength in microns. The data were supplied as relative photon response compared to the peak at 15 µm. In this plot, the data have been scaled so that the 22 µm response is equal to .42, based on results reported by Hughes.
Figure 1.6. Wire bond diagram for the CRC 444A readout (figure courtesy Hughes). This shows the electrical connections between the readout and chip carrier. The number on each pad corresponds to the connection number on the readout. The pads are marked with the following symbols: "V" - bias voltage, "φ" - clock (address or reset), "SG" - system ground, "RG" - reference ground, "O" - output, "N/C" - no connection. The length of the readout is 332 mils, the size of the cavity in the chip carrier where the readout is mounted is 430 mils, and the pixel size is 100 µm.
Figure 1.7. CRC 444A Decoder (figure courtesy Hughes). Four of the eight row address lines are connected to each pixel's readout. When the correct address for a given row is selected, it enables the output reset pulse for the pixels in that row. These are connected to the unit cell (see Figure 1.8).
Figure 1.8. CRC 444A unit cell and detector (figure courtesy Hughes). The ENABLE and RESET clocks are from the CRC 444A decoder (see Figure 1.7). When the pixel is addressed, the ENABLE clock connects the pixel to the output for that column, and the RESET clock is allowed through. There is a separate unit cell circuit for every pixel, except for the components inside the dashed boxes, for which there are 20 in total, one for each column. The "Current Mirror/Output Driver" is on the readout, and the "Typical Output Load Circuit" is on the preamp card.
Figure 1.9. MIRAC block diagram. The diagram is divided into three main sections as indicated by the dashed lines: the cryostat, the electronics at the camera, and the equipment inside the telescope control room. The items in the cryostat section are all the components that are inside the dewar. In the electronics section, the functions in the signal processors and controller board are shown, and these are enclosed by the dotted rectangle. There are ten identical signal processor boards, each with two channels. One is shown in the diagram. Nine clock signals and 14 bias voltages are supplied by the electronics to the detector. Twenty outputs, one from each detector column, are amplified by 4 and enter the inputs of the signal processor boards. The data are transferred to the controller via a 28-bit parallel bus, and are sent to the computer to a 1.25 Mbit/sec serial Manchester transmission line. Commands are also sent from the PC to the camera over this serial line to set the camera parameters. Analog signals from the temperature controller are read by an A/D board inside the PC, and the PC sends commands to the filter motor controller via a RS-232 serial link.
Figure 1.10. MIRAC Bias supply representative circuit. For ISS1, ISS3, and VDET, an additional series resistor is added at the point marked (R5) on the right side of the diagram.
Figure 1.11. Preamp circuit diagram. There are four preamp boards, with five channels on each board.

1.11a. Preamp main circuit. The circuit enclosed by the dotted lines in the lower left for the offset bias is only installed on the first preamp board. The five inputs JA-JE are subminiature connectors where the coaxial cables that carry the detector output are attached.
Figure 1.11b  Preamp circuit, signal reference and power supply bypassing. The signal reference circuit is implemented on circuit board 2 only.
Figure 1.12. MIRAC Controller block diagram. On the left are the connections to the computer, the command and data lines which are serial transmission lines, and IMGRDY which is a logic level. The Serial Encoder/Decoder decodes command words sent from the PC and received by the Manchester serial encoder/decoder. The command word is separated into command and data segments and sent to the command decoder and registers. There are two types of commands, one which performs a function, such as to START imaging, and another which loads a camera parameter register with a data value. The values in these parameter registers specify how the controller timing operates. Control signals are sent to the signal processors, and address and reset signals are sent to the detector.
Figure 1.13. MIRAC PAL timing diagrams. The timing for the section labelled "PAL1" refers to U215 (PAL16R8), and "PAL2" is U216 (PAL22V10). The inputs to both PALs include BITCLK, PIXWAIT, and SMODE00 and SMODE01. BITCLK is the counted-down master clock, PIXWAIT is a control line that can be used to stop some of the PAL output, and SMODE00 and SMODE01 determine the sample mode.

1.13a. PAL1 timing. When PIXWAIT is high, the outputs have the following values: DRST/ = High, CVRT/ = High. The others are unchanged.
Figure 1.13b. PAL2 timing, single sample mode. PAL2 has several inputs in addition to the ones common to all PALs: CT0-CT4 from PAL1, and IMAGING. When PIXWAIT is high, or IMAGING is false for any of the sample modes, the outputs have the following values: COADST, COADDA, COA8A, COA7A, COA6A, OFFBLK1A, OFFBLK0A, and CLMP = low, ADDSUBA = high.
Figure 1.13c. PAL2 timing, double sample mode. See caption to Figure 1.13b.
Figure 1.13d. PAL2 timing, delta reset mode. See caption to Figure 1.13b.

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<td></td>
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Figure 1.13e. PAL2 timing, triple sample mode. See caption to Figure 1.13b.
Figure 1.14. MIRAC Coadder Memory Map. This shows the segmentation of the memory space where the coimage is stored during an integration. Two of the above segments exist on each SP board, one for each channel. The channel is selected with the COA8A address line.
Figure 1.15. MIRAC Signal processor block diagram. The inputs on the left edge of the diagram are from the Preamp outputs. All the addresses and timing signals are from the controller, except for the end of conversion (EOC) signal from the A/Ds, which insures that the data words from the A/Ds are not used before it becomes valid. The data is transferred to the controller from the FIFO memory output bus, shown in the lower right corner.
Figure 1.15

MIRAC SIGNAL PROCESSOR
Figure 1.16. Typical analog output from the detector column, shown at the preamp output. This trace is labeled "1". The trace labeled "2" is the CONVERT pulse on the signal processor. The second pixel is being illuminated by a pinhole source, the other two pixels show the background level and the reset feedthrough. The following sample positions are labeled for the first pixel: A - before reset, B - during reset, and C - after reset. The spike at B is referred to as the reset feedthrough. The horizontal axis scale is .5 usec per division, and the vertical scale is 1 V per division for trace 1 with zero at the top, and 5 V per division for trace 2 with zero at the bottom.